LOW SUPPLY VOLTAGE, LOW NOISE FULLY DIFFERENTIAL PROGRAMMABLE GAIN AMPLIFIERS

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Abstract

This paper presents the architecture, methodology, circuit design technique and measured results of a low voltage (2.6 V), fully differential, low-noise, programmable gain "microphone" amplifier, differential bandgap reference and low-voltage programmable gain "power" amplifier. They can be used in a low supply voltage analogue front-end for digital voice terminals. CMOS technology with $1.2\mu m$ *channel length is used. The measured equivalent average input referred RMS noise voltage of the microphone amplifier is* $5.1nV/\sqrt{Hz}$ *in the voice band at 40 dB closed loop gain. The power amplifier is capable of driving* 50Ω *load 200mV from both supply voltages with distortions better than* 0.5% *under all conditions.*

1 Introduction

Battery operated digital voice terminals need a single low operating supply voltage and low power consumption [1]. Figure 1 shows a typical block diagram of a system. To reduce the number of external components and/or functions and to be able to provide appropriate signal levels for optimum usage of a $\Sigma-\Delta$ A/D converter's dynamic range due to different transducer characteristics, a fully differential programmable analogue front-end with transducer interface modules must be integrated. Among the modules which are hardest to design under the low-voltage and low-power constraint using standard double metal double poly $1.2\mu m$ CMOS technology with a typical threshold voltage of 0.7 V are a low-noise programmable gain microphone amplifier and a power buffer. The programmability of the analogue front-end offers the possibility of hands free operation of the hand-set under software control.

Low supply voltage and the coexistence of a sensitive analogue front-end with a large and fast digital network dictate a fully differential structure, because of critical requirements on PSRR, CMRR and dynamic range. This is because under the low-voltage constraint cascoding is not possible if the typical threshold voltages are about 0.7V. Thus, a fully differential structure and long channel devices used in the gain stages are the only possibilities of maintaining the performances. Moreover, process variations have a large influence on the system behaviour if the design approach is chosen incorrectly. For example, the offset voltage of the microphone amplifier amplified by 40 dB maximum gain reduces the useful dynamic range of the A/D converter that follows the amplifier, so careful circuit and layout design techniques are necessary to minimize these effects. The second important design constraint is the 1/f and thermal noise coming from the microphone amplifier because of its high closed loop gain. It can be shown that the noise performances of the realized amplifier are at the limit of what is achievable in CMOS technology. The offset voltage and noise are not critical parameters for the on chip power buffer because of low closed loop gain. Driving a 50Ω load at low supply voltage and at low power consumption presents a real challenge. A well-known class AB, single ended structure [2] is extended to a fully differential topology. The combined P and N channel differential stage used in a fully differential structure with accurate common mode output balance [3] and quiescent current control circuitry solves the very demanding requirements at low supply voltage in a new way.

In Section 2, we present some problems and possible solutions associated with the low-voltage analogue CMOS circuit design, dealing with bias, band-gap reference, low noise amplifier and power buffer. A list of design considerations relevant to low supply voltage analogue design is added at the end of section 2. In sections 3, 4 and 5, we present circuit design, layout and measured results for bias and references, low noise microphone amplifier and power buffer respectively.

2 Low voltage analogue circuit design: problems and solutions

The operation of an analogue and mixed signal integrated circuits becomes problematic if the supply voltage is reduced: the bandwidth and slew rate of the operational

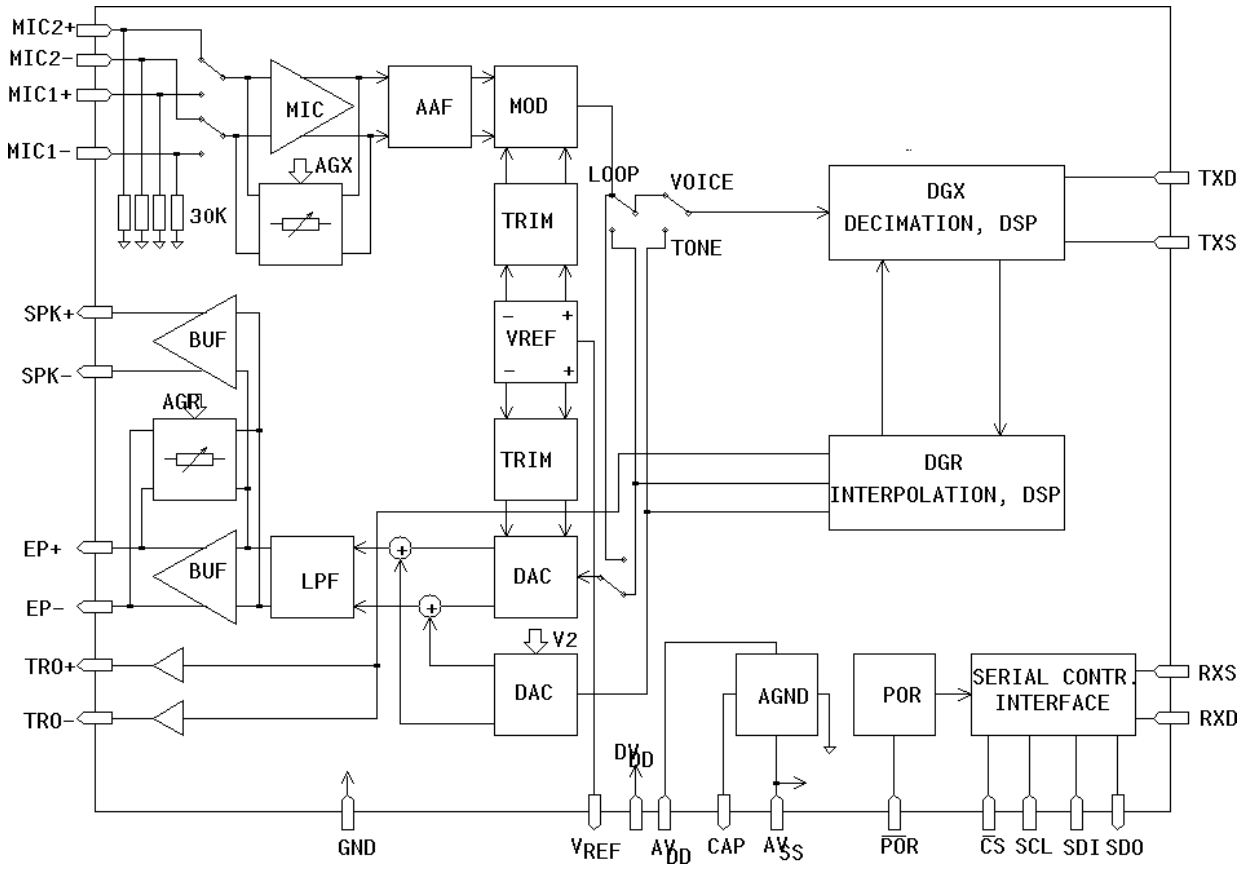

Figure 1: Block diagram of a typical voice interface

amplifier is reduced, the switch on resistance increases, the dynamic range of the A/D and D/A converters is reduced, the stability is harder to control etc. Cascoding, which is the basic technique for increasing the conductance of the MOS current source, speed and open loop gain of the operational amplifiers, can no longer be used. For example, the minimum supply voltage needed for proper operation of a regulated cascode current mirror [4] must be greater than $Vsupp \geq V_{th} + 2V_{dssat} = 1.1V$ using standard CMOS technology with $V_{th} = 0.7V$. Another problem is the variance of the drain current due to threshold voltage variations of two matched current mirrors when they operate close to the moderate or weak inversion regions, which may happen because of a low supply voltage. Another problem is temperature variation and, because of that variation of the key parameters of the MOS transistor. Since cascode transistors cannot be used, a long channel device is the only option for the gain stage to achieve open loop gain, PSRR and CMRR. The noise of the critical opamp must be reduced to retain the required dynamic range. Another problem is the coupling of "digital" noise entering the sensitive analogue paths from the large digital portion of the chip. To overcome these problems, the following design techniques were used: fully differential structure from the microphone amplifier to the modulator, D/A converter and "power" buffer, electrically symmetrical layout, a design technique which keeps all the signals always in the optimal voltage range, appropriate biasing, gain bootstrap, quiescent power control circuitry for power buffers, careful circuit and layout design technique for noise reduction, shielding of sensitive analogue paths, separation of supply lines for sensitive analogue and digital portions of the front-end and appropriate supply of the mixed signal modules such as modulator and the D/A converter, etc.

2.1 Bias and voltage reference

Bias circuit is an important module for proper operation of the analogue front-end at low voltage. To satisfy the requirements over temperature and process, the bias current

should be constant or slightly increasing with temperature to compensate for example mobility degradations [5]. Pure PTAT behaviour using compatible-vertical-bipolar transistors is minimized by using a polysilicon resistor. The nominal base-emitor voltage depends on the selected emitor-current and its absolute value depends on the temperature range of operation. To guarantee as low supply voltage as possible for a given technology, simple low voltage current mirrors in the collectors are used. The right choice of transistor channel length for the current mirrors is important if we know that central bias generator does not need to be very accurate. If the system needs an accurate absolute value of currents, they have to be generated from a stable voltage source (bandgap). Figure **??** shows a simple bias circuit, which requires a minimum supply voltage greater than (equation 1):

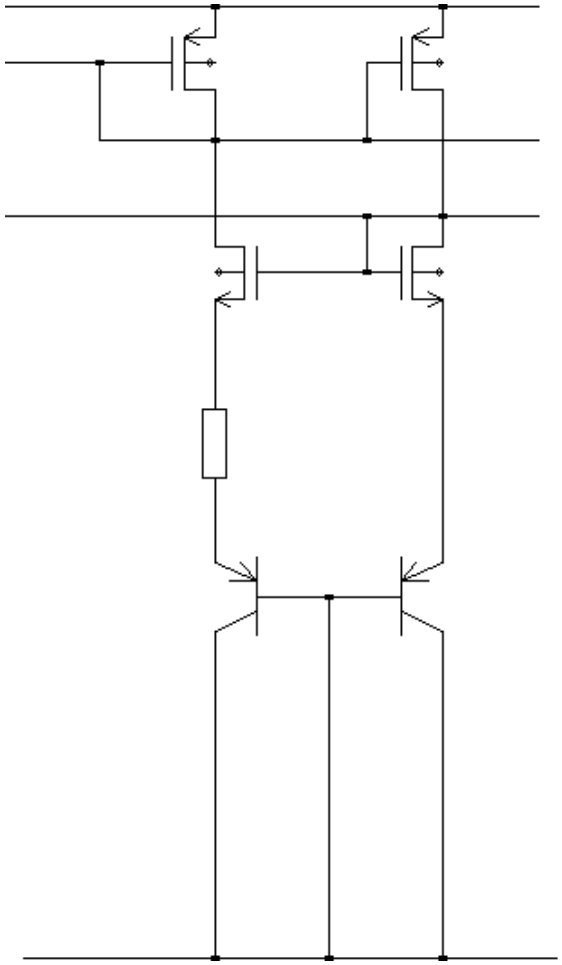

Figure 2: Simple bias circuit

$$V_{s_{min}} \geq V_{th_{max}}(T) + V_{be_{max}}(T) + 2\left(\sqrt{\frac{2I_b}{\mu C_{ox}\frac{W}{L}}}\right) \quad (1)$$

The maximum V_{be} voltage depends on the transistor current I_b and the lowest temperature required, which is also the most critical parameter. To achieve low voltage operation, the current I_b must be small and the (W/L) ratio of the MOS transistors large. A short channel MOS transistor has a lower threshold voltage, but this parameter must be used with caution because of PSRR problems.

The analogue front-end in the presented design operates with a symmetrical reference voltage of $\pm 0.6V$ around ground level, which is fixed in the middle of the optimal operating supply voltage. The bandgap reference (figure **??**) is built of CMOS compatible vertical-bipolar transistors and MOS current mirrors with geometry and current values that minimize the noise energy in the audio frequency band and is capable of operating at a supply voltage down to $2.6V$. The temperature coefficient achieved is smaller than $\pm 40 ppm/^oC$ and the average RMS noise voltage is smaller than $200 nV/\sqrt{Hz}$ in the voice band.

2.2 Operational amplifiers

The following design considerations were taken into consideration during the design of the low supply voltage operational amplifiers used in the presented analogue front-end:

- A fully differential structure helps to maintain the dynamic range and reduce the crosstalk from the noisy substrate if the layout is electrically symmetrical.
- Long channel load devices are used to keep the required PSRR and crosstalk.
- A class A output stage is used in the opamp for the modulator because of the low supply voltage and to keep the linearity of the converter; because of which the quiescent supply current for the modulators opamp is about $150\mu A$.
- cascode transistors are not used for the reasons explained earlier.
- "Low voltage" current sources are used to enhance the voltage swing.
- To keep the noise level low at low supply voltage, a simple resistive common mode detector with linear characteristics is used.

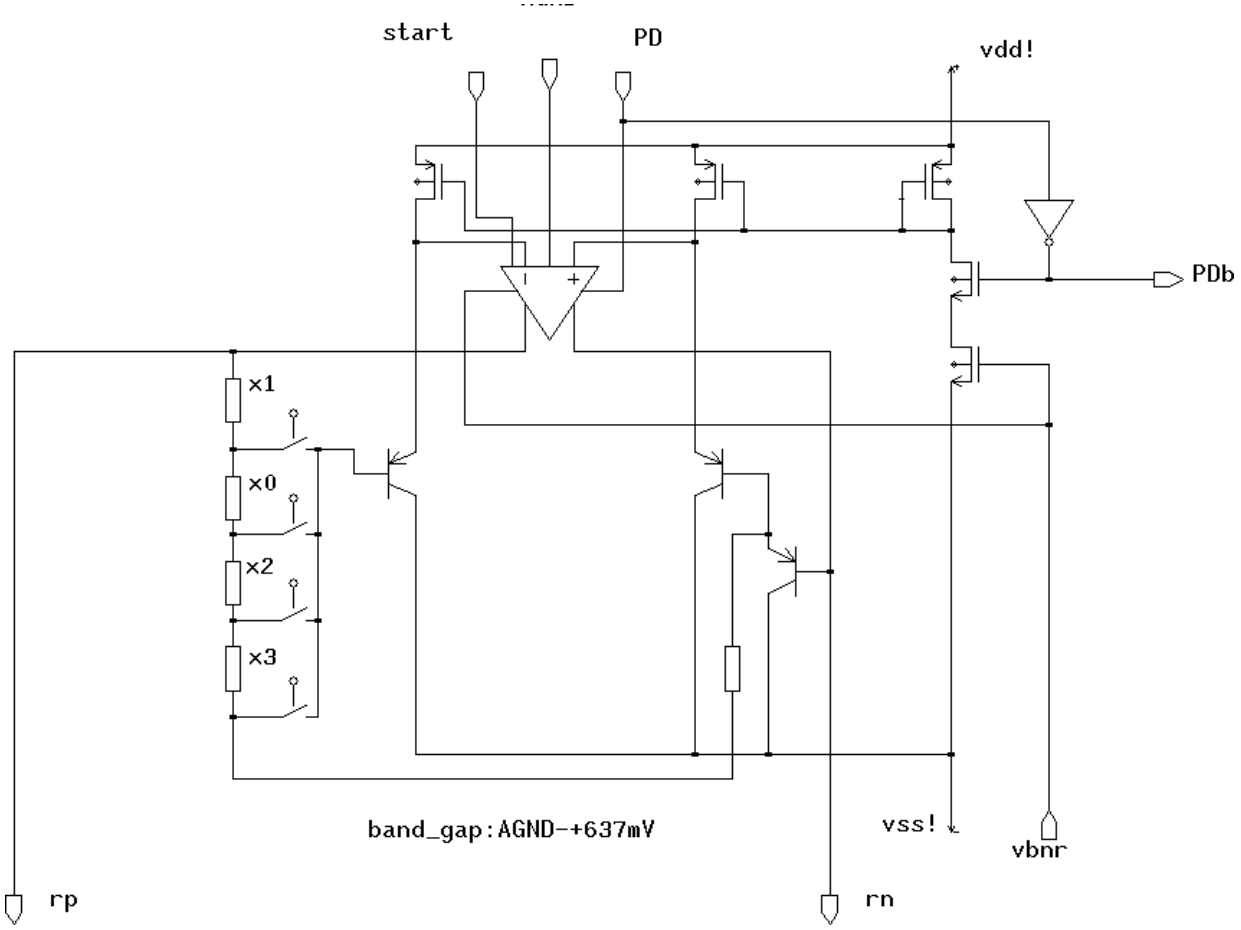

Figure 3: Fully differential bandgap reference

- A simple structure is proposed for the common mode feedback circuit [3]. The common mode and input path have a similar bandwidth. Both signals are added in the common load devices.

- A microphone amplifier with high impedance inputs and precise gain factor is realized by extension of the opamp concept featuring two differential, single channel inputs (so called DDA amplifier) [6]. Special care was taken to enlarge the input common mode range, input voltage range and to reduce the offset voltage and noise.

- If a large input swing is required as in an output buffer, two complementary MOS input stages are used.

- A well controlled quiescent output current is an important function when designing the class AB output stage. Simple current amplifiers control current variations with variations of supply voltage, temperature and process.

3 Programmable gain low noise microphone amplifier

3.1 Circuit design considerations

Figure **??** shows the circuit diagram of a low noise microphone amplifier. The programmability is achieved by using two matched arrays of resistors and switches that are controlled by digital signals. The gain can be varied from 10 dB to 40 dB in 6db steps (Figure **??**). The transconductance of the input stage must be as high as possible for low distortions and low noise. Appropriate layout improves the matching of input and load devices, which contributes to lower distortions. A fully differential structure was used for

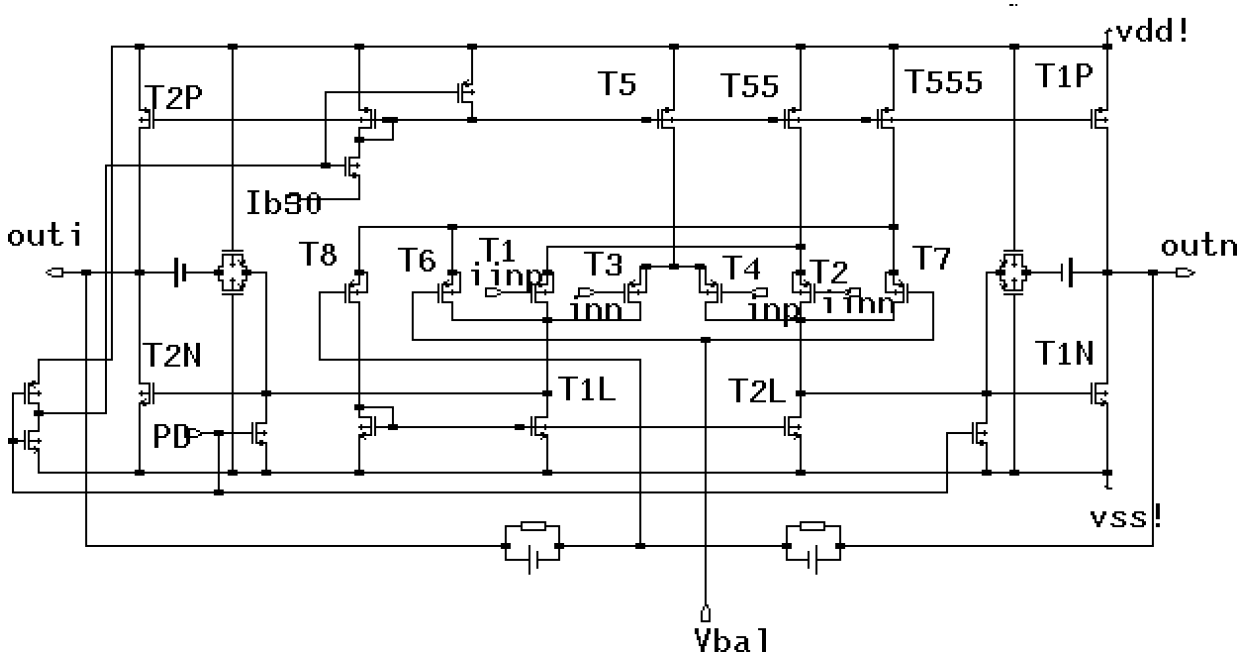

Figure 4: Microphone amplifier schematic

the reasons explained earlier. The achieved performances are summarized in Table 1.

The most critical design parameters are: equivalent average input refered rms noise voltage at 40dB closed loop gain, accurate gain steps of 6dB and accuracy of the gain. Careful layout design technique of the resistor strings and appropriate open loop gain of the amplifier helps to achieve the last two requirements, while the first is realised by an appropriate circuit design technique described in the next subsection.

A psofometrically weighted S/N ratio of 86.5 dB at the output of the microphone amplifier is required for 14 bits resolution of the modulator. This can be achieved if the equivalent input referred average RMS noise voltage of the microphon amplifier is smaller than (equation 2):

$$V_{noise} \leq \frac{V_{mod_{max}}}{G_{mic}\sqrt{BW}10^{\frac{S/N}{20}}} = 5.1\frac{nV}{\sqrt{Hz}} \qquad (2)$$

where : $V_{mod_{max}} = 0.6V_{rms}$, $G_{mic} = 100$, $BW = 3.1kHz$, $S/N = 86.5dB$, It is very hard to achieve $5.1nV/\sqrt{Hz}$ noise voltage using CMOS technology. For comparison, a simple $1k\Omega$ resistor produces approx. $4nV/\sqrt{Hz}$ thermal noise voltage at 25^oC and it is known for a MOS transistor that its 1/f noise contribution is bigger and harder to control than thermal noise in the specified frequency bandwidth.

Each input transistor participates to the equivalent input referred noise voltage by adding its noise power. Noise spectral density at the output is related to the closed loop gain setting and the transfer function of the operational amplifier. Two identical input pairs contribute 3dB higher noise than a single-input stage pair. The common mode feedback stage has a resistive noise source connected from the amplifier output (common mode feedback detector), which is compressed by the amplifier gain, so it can be neglected if the closed loop gain of the amplifier is small. A common-mode amplifier differential pair is 6dB less noisy than an ordinary input pair, because the devices have twice the size and current of the input pair. Common load devices contribute to noise with their transconductances related to input devices. The device area ratio, conductance factor μC_{ox} and N or P type flicker coefficient difference, define the actual noise performance. It is possible to design CMOS input stages with small 1/f and thermal noise in a specified voice frequency range. Resistor strings and input switches add their noise power to the total noise power. The contribution of resistors is different for different gain settings. Table 1 gives important characteristics of the microphone amplifier. A relatively large area (layout on Figure **??**) and supply current are needed to achieve the noise requirements. Figure **??** shows The measured input referred equivalent noise voltage of the microphone amplifier.

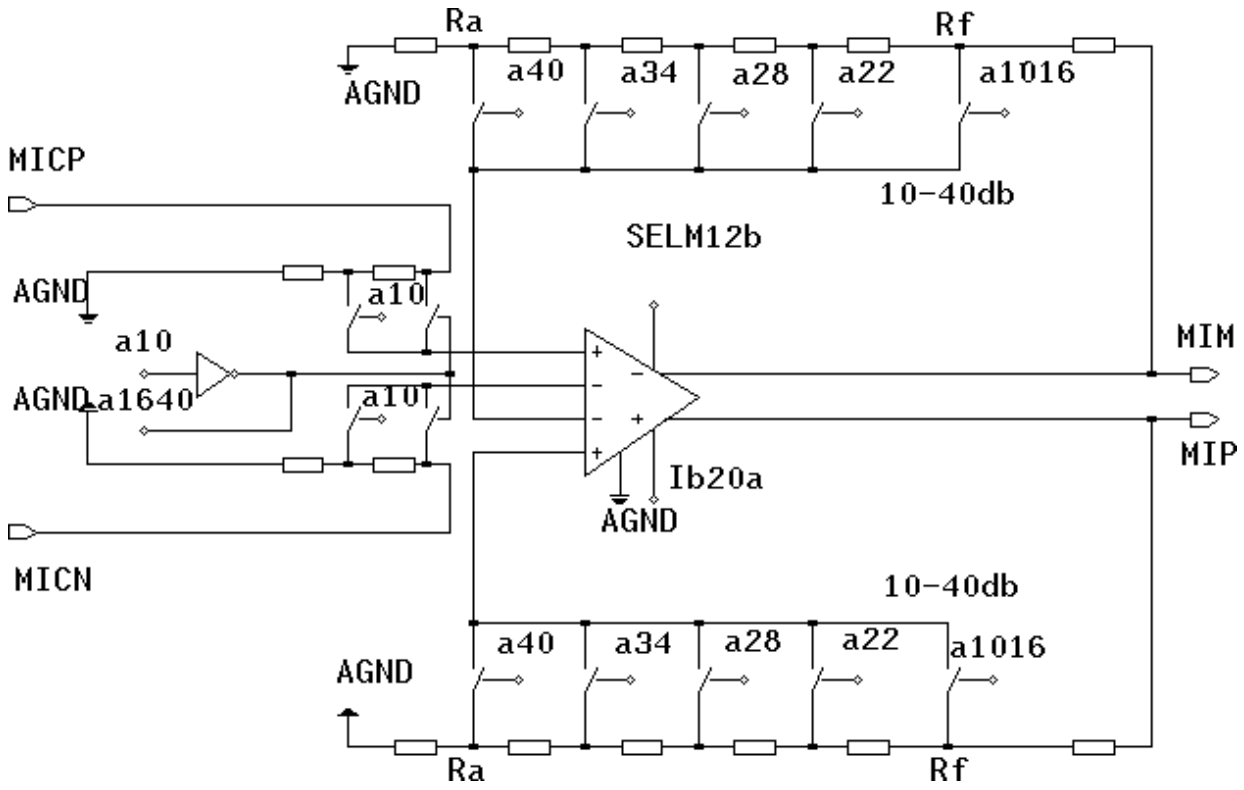

Figure 5: Gain programming circuit

Table 1: Characteristics of the microphone amplifier

Technology	$1.2\mu m$ n-well
V_{sup}	$\geq 2.6V$
$S/N(at40dB)$	$\geq 87dB$
$V_{N_{in}}(300Hz)$	$\leq 7nV/\sqrt{Hz}$
$V_{N_{in}}(1kHz)$	$\leq 6nV/\sqrt{Hz}$
$V_{N_{in}}(0.3-3.4kHz)$	$\leq 5.1nV/\sqrt{Hz}$
$HD(0.2Vp)$	$\leq -52dB$
$\epsilon_{A_{cl}}$	$\leq 0.05dB$
$PSRR(1kHz)$	$\leq 75dB$
I_Q	$\leq 2.6mA$
A	$1.1mm^2$

3.2 Noise reduction technique

Minimizing the gate length L and maximizing the available DC bias current of the first stage devices (transistors T_1, T_2, T_3, T_4 from Figure **??**) reduce the thermal noise. The transconductance of the transistor (T_5) is selected in such a way that its thermal noise contribution is minimized according to relation 3:

$$v_e^2 = A\frac{I_b}{g_m^2} \tag{3}$$

where I_b represents the noise current associated with the current source transistor of the differential stage. The 1/f noise contribution of T_5 is minimized by choosing as large as possible a gate length. Other noise sources, such as parasitic noise due to poly gate with resistance $R_{poly} = 4KT1/R_g$ and substrate with resistance $R_{sub} = 4KT1/R_b$, were minimized by a proper layout. The input stage is designed as common centroid geometry with gates connected from both sides by metal wire.

The substrate contributes to the noise power with substrate resistivity (n-well) and substrate transconductance (the substrate should be connected to a voltage potential which is as far away as possible from the transistor source). If the substrate is connected to the supply, it has constant resistivity, but couples substrate noise to the input stage. So for a high gain and low noise amplifier operating on a noisy substrate, the input transistors substrate must be connected to its own source. Furthermore, resistive underpasses in the signal path to the amplifiers input should

be avoided. The noise contribution of all other transistors in the amplifier should also be considered and optimized, because their noise contributions are not negligible. However, the actual sizes of input and load devices are the function of input voltage range, amplifier bandwidth, stability, and noise requirements. Unfortunately, some effects are in contradiction; for instance, decreasing the input transistor channel length decreases thermal noise but lowers the available input voltage range. The overall noise spectrum of the continuous time amplifier is a function of the close loop gain structure (Figure **??**). Squared average RMS noise voltage on each amplifiers output is (Equation 4):

$$\begin{aligned} \overline{e}^2_{eq}(f) &= 2kT\Big[A^2_{cl}(R_a \parallel R_f) \\ &+ \big(1+A_{CL}\big)^2\big(R_{eq}+2\sqrt{(2)}R_{on}\big)\Big] \end{aligned} \quad (4)$$

where R_{eq} is amplifier equivalent input noise resistor, R_a and R_f are close loop gain setting resistors, R_{on} is switch resistivity (two switches are simultaneously on). All other switches are in the off state and are supposed to be ideal open-circuit. The close-loop gain setting leads to variable values of R_a and R_f and therefore contributes nonconstant noise power to the amplifier input. A low value of R_a means a lower thermal noise contribution of the resistive network $R_a||R_f$. In general, for low noise power, low resistances R_a, R_f and R_{eq} are required. The noise coming from the gain adjust MOS switches is simply a function of on resistance of the switch, ie the transistor in its linear region of operation. It is a function of the effective gate voltage V_{eff}.

$$e^2_{sw}(f) = 4kTR_{on} = \frac{4kT}{2\big(\frac{W}{L}\big)\mu C_{ox}V_{eff}} \quad (5)$$

Equation 5 gives the squared RMS noise voltage of the switch normalized to the 1Hz bandwidth.

4 Class AB fully differential driver

A schematic diagram of a class AB differential output driver is shown on Figure **??**. The speed of this driver is not very demanding, so its major drawback, which is the slew rate limited differential stage, does not really matter. The hardest design requirement is a driving capability of 50 Ω and $4V_{p-p}$ output signal at 2.6V supply voltage with $HD \leq 0.6\%$ under all conditions and with as small a quiescent supply current as possible. The input voltage range of the amplifier, if used as a unity gain buffer, must be as close to the supplies as possible. For that reason, two complementary differential input stages are used. The common mode input range is symmetric about the analogue ground voltage. Input voltage range is limited to V_a (equation 6) and V_b (equation 7),

$$V_a = V_{dd} - \sqrt{\frac{I_b}{\mu C_{ox}\big(\frac{W}{L}\big)_{L_P}}} + \mid V_{th_{L_{p_{max}}}} \mid + V_{th_{D_{n_{min}}}} \quad (6)$$

$$V_b = V_{ss} - \sqrt{\frac{I_b}{\mu C_{ox}\big(\frac{W}{L}\big)_{L_N}}} + V_{th_{L_{n_{max}}}} + \mid V_{th_{D_{p_{min}}}} \mid \quad (7)$$

where I_b is the input transistor current, $V_{th_{L_{max}}}$ and $V_{th_{D_{min}}}$ are threshold voltages of load (L) and differential (D) transistors.

Common mode amplifier, built of transistors T_3 and T_4 and equal to the main differential stage, controls the common mode output voltage. It is responsible for small signal output performances and amplifier stability. A resistive divider connected to both outputs on one side and to the gate of transistor T_3 on the other side closes the common mode feedback loop and, as a consequence, the common mode output voltage is very close to the input balance voltage connected to the gate of transistor T_4. The resistive divider is used to keep the loop in a linear mode over a large output voltage range. Differential and common mode gains are similar because of the same transistor sizes, similar currents and common load devices; for the same reason, the amplifier needs only one compensation network for each output. Additional bias current is added to the load devices to avoid an unbalanced condition if the input stages are turned off. Both transistors of the AB class output stage are driven directly from the differential stage. The maximum output voltage swing is (Equation 8):

$$V_{ss} + \sqrt{\frac{I_N}{\beta_N}} \leq V_o \leq V_{dd} - \sqrt{\frac{I_P}{\beta_P}} \quad (8)$$

where $\beta_N = \mu C_{ox}(W/L)_N$ and $\beta_P = \mu C_{ox}(W/L)_P$. Both output transistors are optimized for maximum transconductance and are suitable for driving large capacitive and low resistive loads. The quiescent current is measured in the crossover region for each output transistor and compared to the predetermined bias current [2]. Perfect matching of all four control circuits is not necessary because they all use a stabilized and equal bias current level. The total supply current variations with temperature, process and supply, taking into account a 10 mV random offset voltage variation, is 15% over a wide supply voltage range (2.8 V to 5 V). To equalize HD with temperature, a modified PTAT biasing is used. Figure **??** shows the connection of the amplifier. The major drawback of the operational amplifier from Figure **??** is the signal dependent gain (5% over the full range). The reason is transconductance mismatch due to the low channel length of input devices.

Figure **??** shows the layout of the power buffer, while Figure **??** shows the measured output spectrum of the buffer at $V_{sup} = 3V$, balance voltage $V_{bal} = 1.5V$ and differential load is 50Ω or 100nF. The main characteristics of the buffer are presented in Table 2.

Table 2: Characteristics of the power buffer amplifier

Technology	$1.2\mu m$ n-well
$V_{in_{max}}$	rail to rail
$V_{o_{max}}(0.6\%HD)$	$100mV$
$V_{o_{max}}(0.3\%HD)$	$300mV$
I_Q	$3.25 \pm 0.5mA$
$PSRR(1kHz)$	$\geq 78db$
$SR(V_{in} = \pm 1V)$	$2.5\frac{V}{\mu s}$

5 Conclusions

Design considerations and measured results of a low voltage, low noise amplifier and power amplifier are presented in the article. They are used in a programmable analogue front-end for digital voice terminals. A measured equivalent input referred RMS noise voltage of $5.1nV/\sqrt{Hz}$ in the voice frequency band was achieved; this is at the limit for CMOS technology and was possible only by using very careful circuit and layout design techniques. The output buffer is capable of delivering 30mW power into 50Ω load at $3V$ supply and 0.5% HD distortions with the quiescent supply current sufficiently low. The measured results of important parameters for both amplifiers are given in the article.

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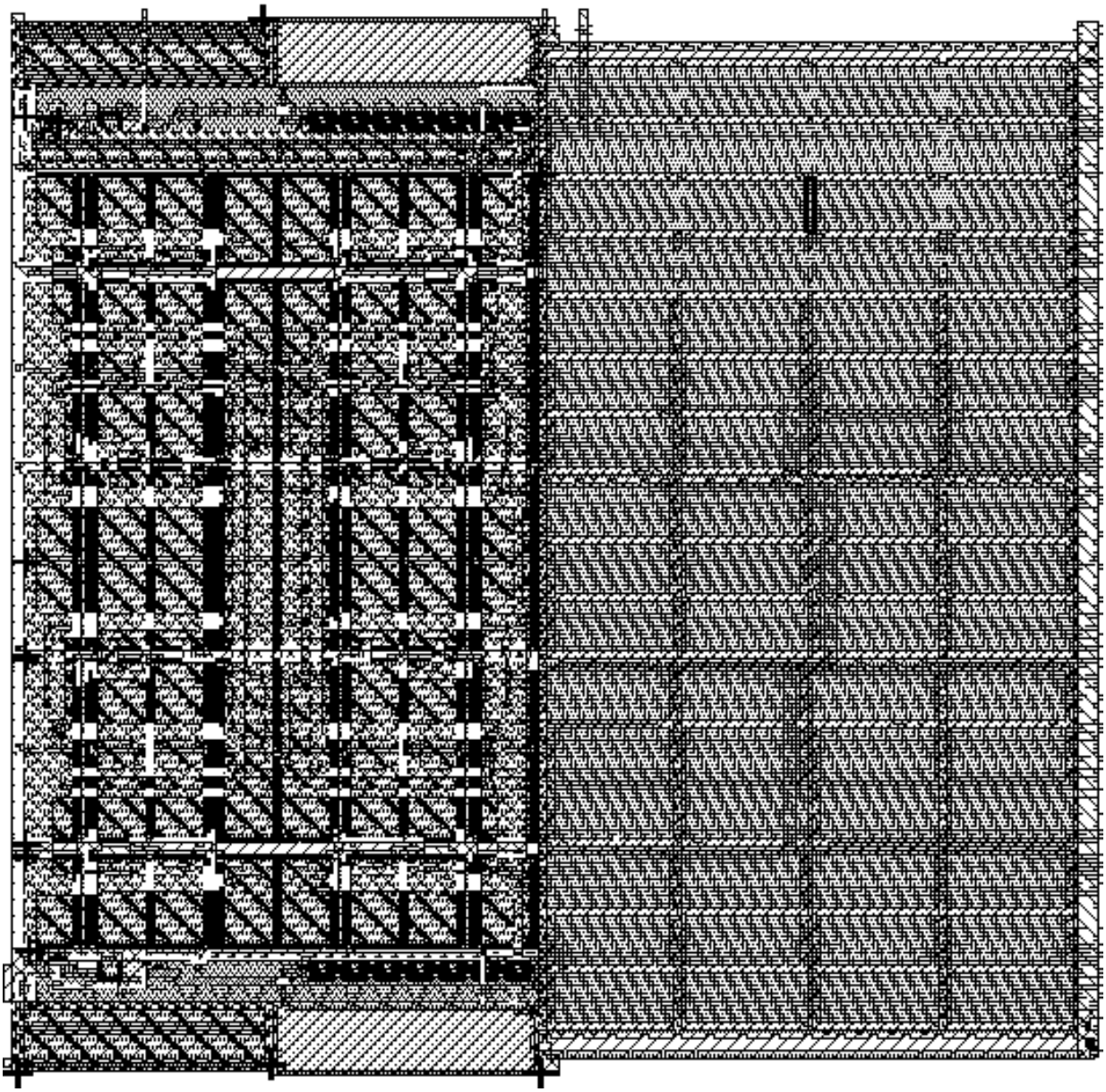

Figure 6: Microphone amplifier layout

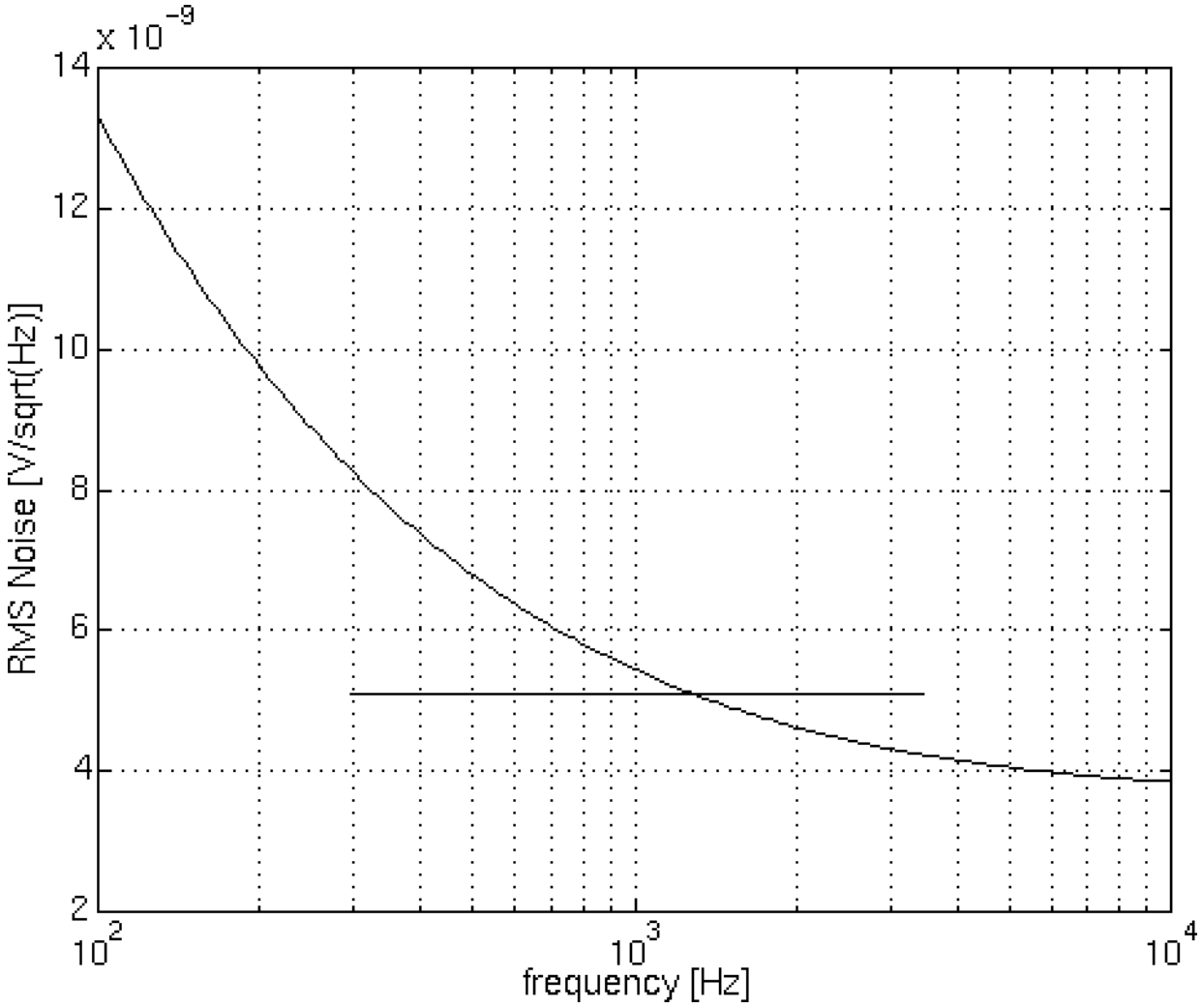

Figure 7: Measured input referred noise voltage of the microphone amplifier at $25^{o}C$

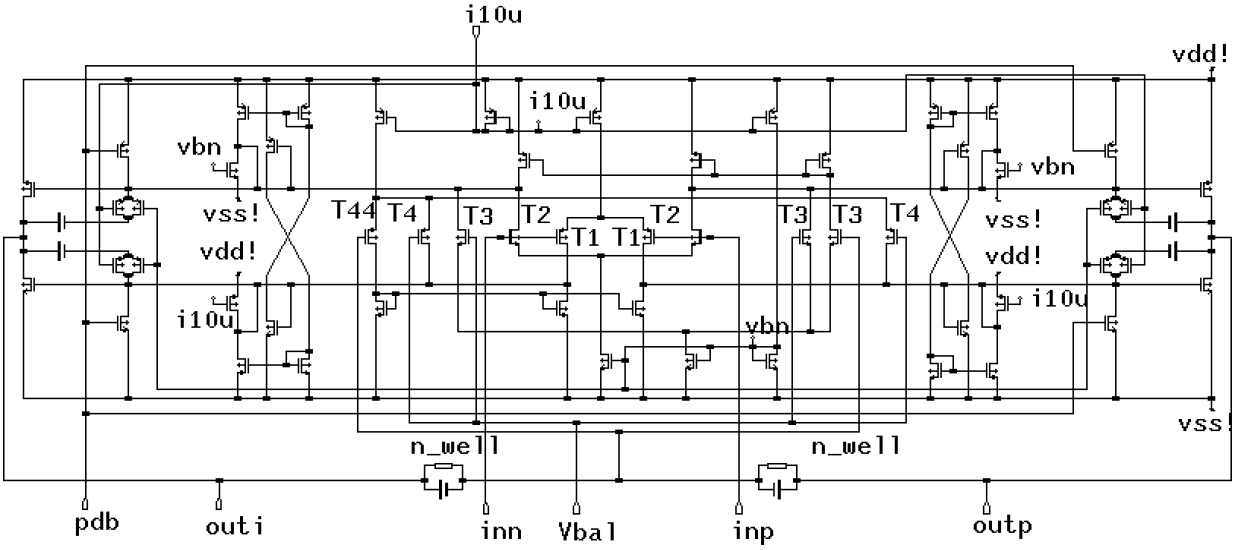

Figure 8: Differential output driver

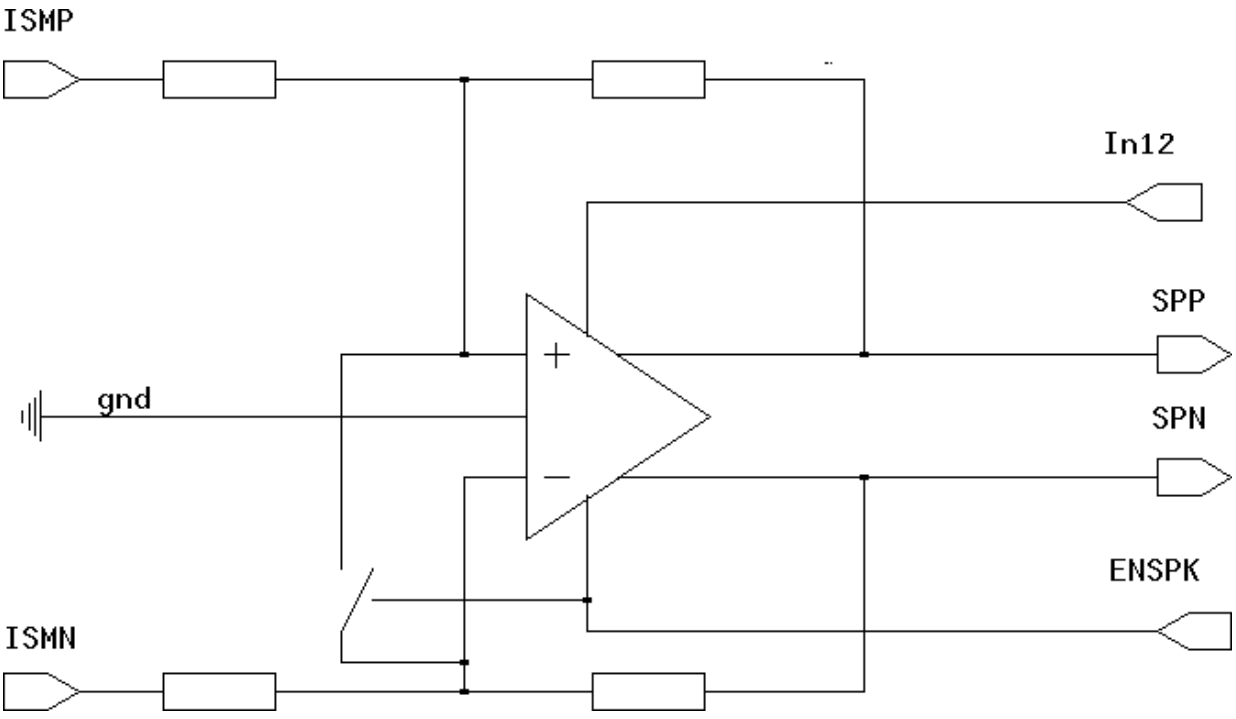

Figure 9: Power buffer as inverting amplifier

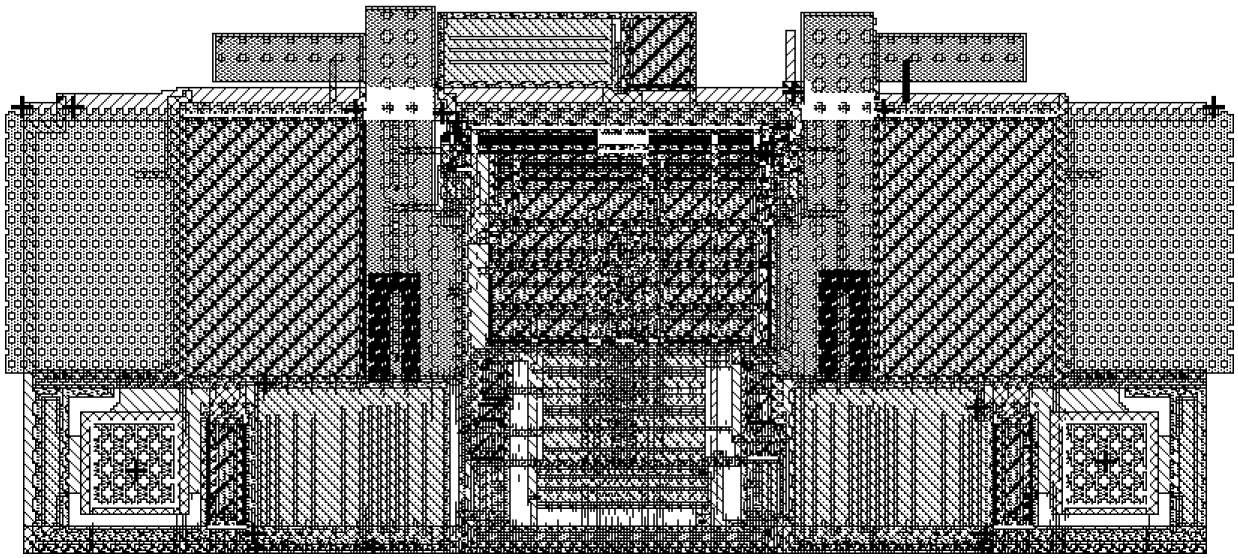

Figure 10: Layout of the power amplifier

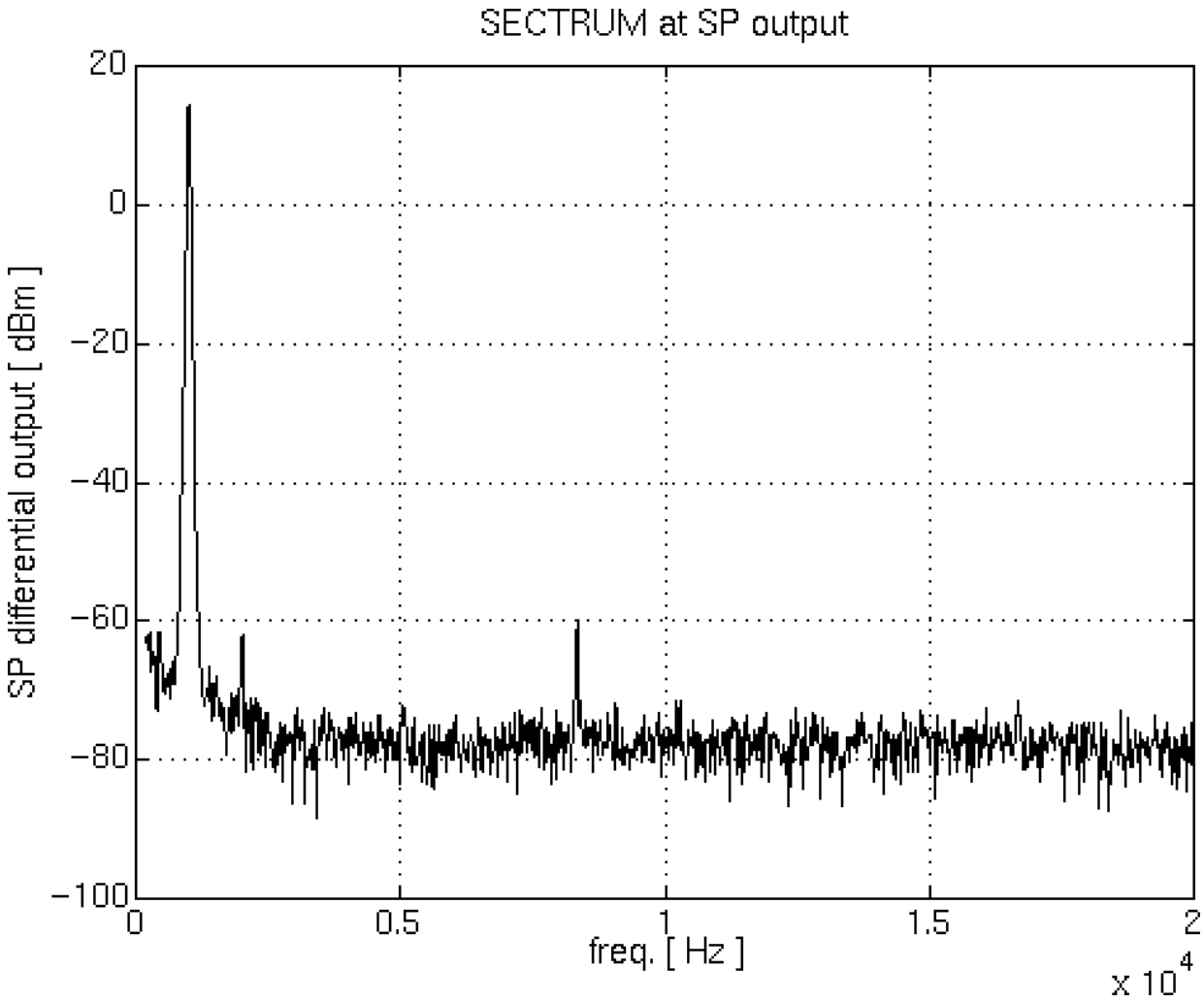

Figure 11: Output spectrum of the power amplifier