SUBTRACT: A Program for the Efficient Evaluation of Substrate Parasitics in Integrated Circuits

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***Abstract*—Algorithms for the efficient evaluation of substrate parasitics in mixed-signal integrated circuits have been developed and incorporated in an extraction tool for substrate parasitics, SUBTRACT. Using a preprocessed, polynomial-based boundary element method, SUBTRACT enables the parasitic extraction process to be completely technology independent, allowing for fast evaluation. Additionally, techniques to accelerate the iterative solution of the resulting impedance matrix have been developed and employed to further improve the speed advantages that this method offers. The preprocessed boundary element method is more efficient than finite-difference schemes and orders of magnitude faster than general boundary element methods using a direct evaluation of Green's function. Results of employing SUBTRACT to the design and verification of a mixed-signal A/D converter IC are described.**

I. INTRODUCTION

With increasing speeds, shrinking IC technologies, and an emphasis on compactness in consumer electronic products, monolithic mixed-signal integrated circuits are becoming ubiquitous in the semiconductor industry. The design of these circuits is unfortunately becoming an increasingly formidable task owing to various parasitic coupling problems that affect mixed-signal systems. One of the key determinants of performance in modern mixed-signal ICs is substrate coupling, the phenomenon whereby noise injected into the substrate (and substrate power supplies) by switching logic gates can affect sensitive analog nodes on the same die. Rather than adopting a "build it and see" mentality, mixed-signal designers have begun to use substrate parasitics in the electrical simulation of their designs to better predict performance limitations in their designs due to substrate coupling [1],[2].

Several schemes have been proposed for the extraction of substrate parasitics in integrated circuits. Among these, numerical solution of Laplace's equation on the three-dimensional substrate structure using finite difference-based methods has been the most popular [3]-[5]. Finite difference schemes, while attractive for their simplicity of use and versatility in handling virtually any type of substrate profile, are not very useful in realistic mixed-signal designs because the mesh sizes required for *accurate* extraction become too large too quickly, with increasing domain size. Although sophisticated discretization schemes (other than a simple rectangular one) can be used to eliminate the generation of mesh nodes in regions where they are unnecessary, such schemes come at added computational expense.

An alternative scheme for substrate parasitic extraction is the boundary element method (BEM) using Green's functions for a given substrate under suitable boundary conditions. The Green's function is the potential at any point in a medium due to a current injected at any point also in the medium and can be determined for the substrate in quasi-analytical form [6],[7]. The areas of the substrate that connect to the external world (device/contact areas) are discretized into a collection of *n* panels, and the contribution to the potential at each panel due to currents injected at every panel is stencilled into an *nxn* matrix of impedances which is then solved to determine the substrate admittances. This technique is very appealing since it reduces a 3-D problem effectively into a 2-D one. However, a direct evaluation of the quasi-analytical Green's function (a series expansion of hyperbolic sines and cosines) involves several million floating point multiplications and additions and since it must be repeated for every pair of panels, formulation of the impedance matrix becomes an expensive task for large problems. Alternatively, discretizing the entire substrate surface into a uniform grid of panels, a 2-D Discrete Cosine Transform can be utilized to precompute all the panel-to-panel impedances on the substrate in *O(NlogN)* time [7]. Although very useful, an unfortunate consequence of the latter approach is that nonuniform discretization of ports cannot be taken advantage of and the resulting BEM matrix is much larger than required. The modified Galerkin solution procedure utilized in the BEM could also become ill-conditioned because the singularity in current density at port edges cannot be accommodated with uniformly sized panels. Another problem with the BEM approach in general is that inversion of the dense *nxn* matrix is a cumbersome task. Direct LU factorization requires $O(n^3)$ operations which is clearly infeasible for a reasonably sized problem.

In this paper, we describe algorithms that overcome all the limitations of the aforementioned methods. The techniques to be presented have been incorporated in a substrate

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parasitic extraction tool, SUBTRACT. Section II presents a boundary element method which utilizes a preprocessed, polynomial-based model for a given substrate profile to rapidly evaluate panel-to-panel substrate impedances. The polynomial-based model is computed once for a given substrate in a preprocessing stage and can be used repeatedly at a computational complexity that is far lower than that required in directly evaluating the Green's function. The model also allows for nonuniform discretization and since it is generated using a curve fitting technique on a set of data points, a wide variety of input data can be utilized, i.e., the impedance data to the model generator can be results of a Green's function analysis, 3-D finite difference simulation, device-level simulation or even measurements. The latter is particularly useful for substrates that have not been well characterized or are subject to resistivity fluctuations inherent in the process (e.g., upward diffusion of boron in heavily-doped bulks). Section III describes the use of multipole and local expansions for general polynomial-based potentials that accelerate solution of the resulting dense impedance matrix. In Section IV experimental results are presented that verify the superior performance of the algorithms to be presented. Finally, in Section V the application of SUBTRACT to the design and verification of a mixed-signal video A/D converter IC [14] is described.

II. PREPROCESSED BEM

The starting point of the boundary element method is the discretization of the ports in the system into a collection of panels. Since the ports (active areas) on the IC substrate are found only on its top surface (except possibly for a backside contact), the potential at any panel on the top surface due to current injected at any panel also on the top surface (i.e, the panel-to-panel impedance) is a function of only the distance between them. In the presence of a backside contact, the same is true for potentials with respect to the backplane. (Experimental results confirm that the lateral edge effects, i.e. due to the finite chip boundaries in the *xy* plane of the substrate, can be ignored for typical mixed-signal ICs) Consequently, given a set of data points of impedances for different panel-to-panel separations for a given substrate profile, it is possible to generate a set of polynomials that characterize the variation of impedance with respect to separation for all possible separations of interest.

The first step to generating such an impedance model is collecting the data points required for the curve fitting. The data points can be determined using Green's function, 3-D finite difference simulations, device level simulations or from measured data. SUBTRACT accepts either a set of data points or a substrate profile as an input. Given a substrate profile, it invokes a Green's function analysis to precompute the panel-to-panel impedances required in the polynomial model generation phase. The substrate Green's function, $G(x,x',y,y')$, with (x,y) and (x',y') being the coordinate locations of the observation and source points on the substrate surface is:

$$\sum_{m=0}^{M}\sum_{n=0}^{N} f_{mn}\cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{m\pi x'}{a}\right)\sin\left(\frac{n\pi y}{b}\right)\sin\left(\frac{n\pi y'}{b}\right) \tag{1}$$

where f_{mn} for a homogeneously doped substrate is given by:

$$f_{mn} = \frac{C_{mn}}{ab\sigma}\tanh\left(\sqrt{\frac{m^2\pi^2}{a^2}+\frac{n^2\pi^2}{b^2}}\,c\right). \tag{2}$$

$C_{m,n}$ is a constant, σ is the substrate conductivity and (a,b,c) are the (X,Y,Z) substrate dimensions. For a multi-layered substrate profile (of uniform sheet resistivities) a more complicated expression is obtained for f_{mn}.

In the model generation phase, the range of separations of interest are divided into a geometrically progressing set of intervals in each of which a polynomial is curve-fitted. Since the impedance decreases as the separation, *s* between panels increases, a polynomial in *1/s* is used, i.e.,

$$Z(s) = k_0 + \frac{k_1}{s} + \ldots + \frac{k_m}{s^m} \tag{3}$$

where *m* is the order of polynomial generated. If the error in the polynomial generated exceeds a threshold, a polynomial of higher order is fitted and/or the interval size is reduced. The polynomial generation process is repeated for panels of different sizes, although for larger sized panels, the impedances (data points) can be reconstructed from those already determined in a computationally inexpensive manner. Although the expression in (1) is typically evaluated to a high order (M=N=500), since evaluation of the double Fourier series is greatly simplified using a 2-D Discrete Cosine Transform [7], precomputation of the required impedances and curve fitting the impedance model can be done extremely fast. It must be noted however, that the computational expense incurred in the model generation step is immaterial since it is done only once for a given process. Once the impedance model is determined, the corresponding entry in the dense impedance matrix for a given pair of panels is done by merely evaluating the corresponding polynomial.

III ACCELERATED BEM MATRIX SOLUTION

Clearly, a major bottleneck in the boundary element method is the solution of the dense *nxn* impedance matrix. LU factorization as mentioned earlier is infeasible for more than a few hundred panels because of its $O(n^3)$ operation count for a dense matrix. Alternatively, iterative methods in the conjugate-residual style such as GMRES [8] can be employed. To solve the matrix equation, $Zi = v$, these methods minimize

the norm of the residual error (v^k - Zi^k) over a Krylov subspace at every step, *k* in an iterative process.

The major cost of the GMRES algorithm is in initially stencilling the dense matrix *Z* and in each iteration, *k* computing the matrix vector product, Zi^k both of which require $O(n^2)$ operations. From classical potential theory it is well known [9] that it is possible to avoid computing most of *Z* and to substantially reduce the operation count of Zi^k by using an approximation to Zi^k, if tolerable. One such approach is through the use of multipole and local expansions [10],[11]. A multipole expansion is a truncated series representation of the far field potential due to a given current distribution while a local expansion is a truncated representation of the potential distribution at distant evaluation points. The multipole and local expansion technique can be adapted to accelerate computation of general polynomial-based potentials. (Note that potential here refers to the result of the matrix vector product, Zi^k at every iteration in the GMRES algorithm.)

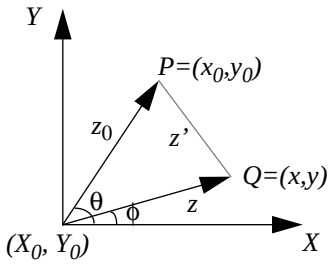

Fig. 1. Points P and Q separated by a distance z' and subtending an angle θ–ϕ between them.

As shown in Fig. 1., for a unit current injected at a point *P*, different from the origin, the potential at a point $Q \neq P$ is dependent on the inverse of the distance *PQ* =*z'*. If $z > z_0$ it can be shown that:

$$\frac{1}{z'} = \sum_{n=0}^{\infty} \frac{z_0^n}{z^{n+1}} P_n(u) \tag{4}$$

where $P_n(u)$ is the Legendre polynomial of degree *n* and $u = cos(\theta - \phi)$. Similarly if $z < z_0$, the potential at *Q* is still described in terms of *1/z'* and can be written as:

$$\frac{1}{z'} = \sum_{n=0}^{\infty} \frac{z^n}{z_0^{n+1}} P_n(u). \tag{5}$$

Equation (4) is called a multipole expansion and equation (5) a local expansion and the truncated series limit is referred to as the order of the expansion. The far field potential at *Q*, v_Q due to a current i_P injected at *P* with the preprocessed point-to-point impedance represented as a *2nd* order polynomial can be expressed as:

$$v_Q(z) = \left[k_0 + \frac{k_1}{z'} + \frac{k_2}{z'^2}\right] i_P \tag{6}$$

where $z' = z - z_0$. Using (4) in (6) gives v_Q as:

$$\left(k_0 + k_1 \sum_{n=0}^{1} \frac{z_0^n}{z^{n+1}} P_n(u) + k_2 \left\{ \sum_{n=0}^{1} \frac{z_0^n}{z^{n+1}} P_n(u) \right\}^2 \right) i_P \tag{7}$$

or

$$\left(k_0 + \frac{k_1}{z} P_0 + \frac{k_1}{z^2}(z_0 P_1 + P_0^2) + \frac{2k_2 P_1 P_0 z_0}{z^3} + \frac{k_2 P_1^2 z_0^2}{z^4}\right) i_P \tag{8}$$

Noting that the Legendre polynomials can be expressed as

$$P_0 = 1; P_1 = cos\theta cos\phi + sin\theta sin\phi \tag{9}$$

and that $zcos\theta = (x-X_0)$, $zsin\theta = (y-Y_0)$, $z_0 cos\theta = (x_0-X_0)$ and $z_0 sin\theta = (y_0-Y_0)$ where (x,y), (x_0,y_0) and (X_0, Y_0) are the coordinate locations of points *Q*, *P* and the origin respectively, substituting (9) in (8) gives the multipole expansion of order 1 as

$$v_Q(z) = a_0 + \frac{a_1}{z} + \frac{a_2}{z^2} + \frac{a_3^0 x}{z^3} + \frac{a_3^1 y}{z^3} + \frac{a_3^2}{z^3} + \frac{a_4^0 x}{z^4} + \frac{a_4^1 y}{z^4}$$

$$+ \frac{a_4^2}{z^4} + \frac{a^0{}_6 x^2}{z^6} + \frac{a^1{}_6 y^2}{z^6} + \frac{a^2{}_6 xy}{z^6} + \frac{a^3{}_6 x}{z^6} + \frac{a^4{}_6 y}{z^6} + \frac{a^5{}_6}{z^6} \tag{10}$$

where the multipole coefficients a_j^l are functions of the impedance polynomial constants k_i and the coordinate locations (x_0,y_0) and (X_0,Y_0) [12]. The far field potential due to several injection points can be expressed as a sum of the individual multipole expansions. The advantage of the multipole expansion becomes clear when the number of injection points exceeds the number of multipole coefficients. Then, rather than directly evaluate the far field potential at each of *m* distant evaluation points due to each of *n* injection points in $O(mn)$ time, a multipole expansion for the injection points can be computed and potentials evaluated with this expansion in $O(m+n)$ time. Similarly, local expansions of polynomial-based potentials can also be developed. Since the impedance model is actually a set of polynomials for different intervals of separations, multipole coefficients must be developed for each interval. The multipole and local expansions can then be employed in a hierarchical fashion to reduce the computational complexity of the matrix vector product in the GMRES algorithm to $O(n)$ [10]-[12].

IV. RESULTS

Both the preprocessed boundary element method and the accelerated matrix solution techniques have been verified with test structures on different substrate profiles [12]. The results of this section have been obtained with the substrate profile of a 1µm n-well CMOS process consisting of a 7 µm thick lightly-doped epitaxial layer (15 Ω-cm) on a heavily-doped bulk (0.02 Ω-cm). Fig. 2. shows the polynomial approximation to actual impedances precomputed for different values of separation using Green's function for two square 10 µm panels. The maximum approximation error in the polynomial model is less than a percent of the corresponding self impedance. Evaluation of the polynomial is several orders of magnitude faster than a direct evaluation of the series of (1).

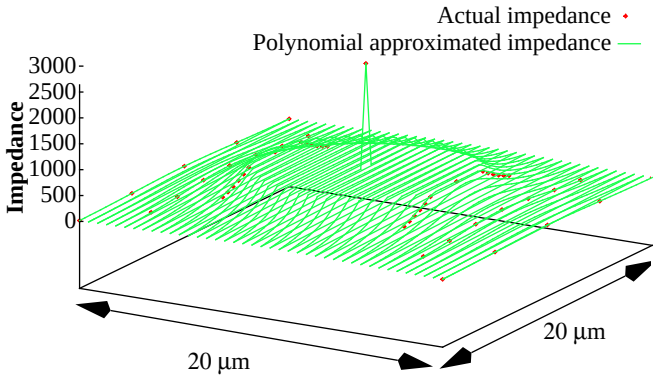

Fig. 2. Polynomial impedance model for two 10 µm square panels.

To verify the effectiveness of the accelerated GMRES algorithm, results using it have been compared to those obtained with both LU factorization and the GMRES algorithm without acceleration. Fig. 2. shows a comparison of CPU times required for extraction using LU factorization and the GMRES algorithm with and without multipole acceleration, as the number of panels is increased.

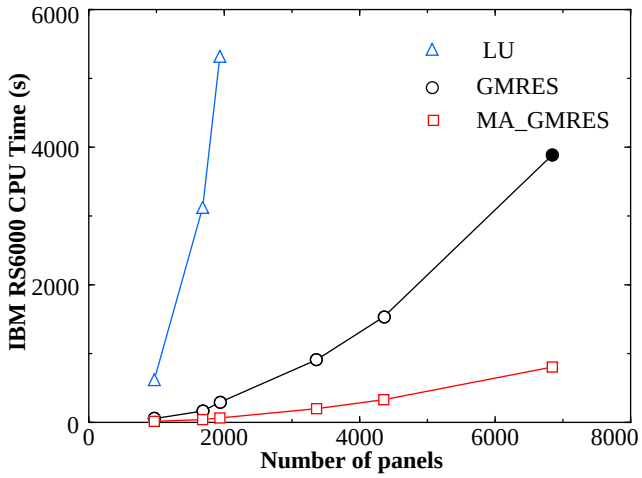

Fig. 3. Comparison of CPU times as a function of the number of panels for LU, GMRES and multipole accelerated GMRES algorithms.

It is apparent from Fig. 3. that the multipole accelerated GMRES (MA_GMRES) method is nearly linear in the number of panels (beyond ~ 2000 panels) while direct GMRES varies roughly as $O(n^2)$ and LU is $O(n^3)$. The last data point on the GMRES curve is an estimated value since there was inadequate memory to store the required impedance matrix. Simulation results using the MA_ GMRES extracted parasitics indicate that a multipole expansion of order 1 is adequately accurate for the substrate problem [12]. The accuracy obtained with the multipole method is illustrated in TABLE I which compares the admittances obtained in a multipole accelerated GMRES extraction to corresponding direct GMRES and LU extracted admittances for a simplified output buffer circuit layout with 8 ports. Node 0 represents the heavily-doped bulk which behaves as a single node [1].

TABLE I Comparison of results obtained using LU factorization, GMRES and multipole- accelerated GMRES methods.

RESULTS	LU	GMRES	MA_GMRES
y_{11}	0.0192	0.0192	0.0194
y_{12}	-8.86e-5	-8.632e-5	-8.95e-5
y_{13}	-4.21e-4	-4.27e-4	-4.43e-4
y_{14}	-3.89e-4	-3.90e-4	-4.05e-4
y_{15}	-1.42e-4	-1.43e-4	-1.48e-4
y_{16}	-8.11e-4	-8.10e-4	-8.31e-4
y_{17}	-3.06e-4	-3.05e-4	-3.17e-4
y_{18}	-1.96e-4	-1.97e-4	-2.03e-4
y_{10}	0.0168	0.0168	0.0170

V. APPLICATION TO IC DESIGN AND VERIFICATION

SUBTRACT has been employed in the verification of a mixed-signal triple 8-b video A/D converter [14] for substrate noise problems. Initial versions of the ADC design displayed several missing code problems and failed to meet the DNL (differential nonlinearity) specification of +/- 0.5 LSB largely because of the switching noise introduced into the substrate by the output buffer and logic circuitry on the IC. Using a hierarchical methodology [12],[13], SUBTRACT was employed to determine a parasitic substrate coupling model associated with this IC. Since the twelve output buffer cells were found to generate much of the switching noise, SUBTRACT was used to determine a detailed parasitic model associated with these cells. The corresponding schematic of the output buffer (and ESD protection circuitry) along with the resistances extracted by SUBTRACT is displayed in Fig. 6. Note that only a few of the significant resistances have been displayed for the sake of clarity. Since the substrate in this

particular IC is a heavily-doped one, the bulk is considered a single node. Simpler models were also extracted for the logic and comparator circuitry on-chip.

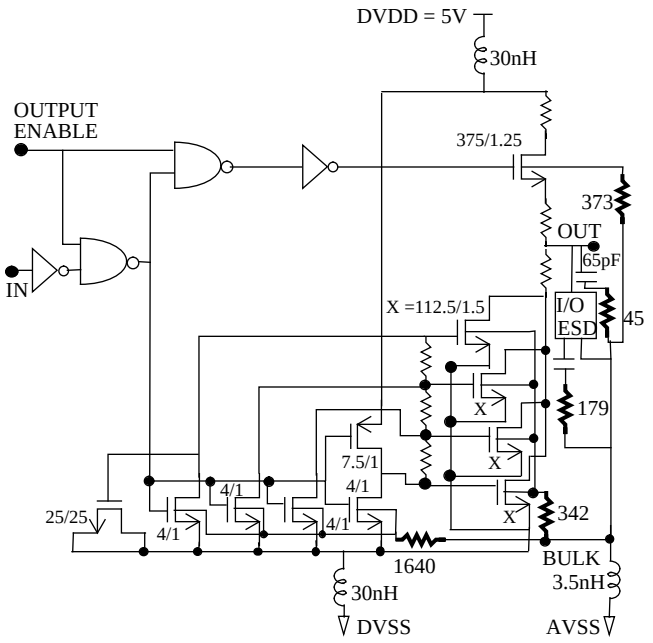

Fig. 4. Circuit schematic of the output buffer and ESD circuitry on the video A/D converter IC. Resistances (in Ω) in bold are extracted by SUBTRACT.

Simulation of the ADC using the substrate parasitic models indicated that the 200mV (peak-to-peak) noise on the substrate was mostly a result of capacitive coupling from the switching output buffers and p-n junction diode (substrate to NMOS drain) turn on due to the associated excessive ground bounce on the DVSS (output ground) line. To overcome the problem several changes were made to the layout and design of the IC. Capacitive coupling to substrate was minimized by routing n-wells under bonding pads and long clock lines and by reducing drain-substrate junction capacitances where possible. Digital supply (DVSS and DVDD) inductances were lowered and the supply lines were resistively damped. The twelve outputs were staggered to prevent their simultaneous switching and the switching characteristics of the buffers were modified to reduce the supply ground bounce. Post redesign simulations indicated that the noise on the substrate was reduced by almost 5X in peak-to-peak amplitude.The chip was refabricated and tested. Measured results from the redesigned IC confirm that it is functional with no missing codes and a DNL error of less than 0.5 LSB.

VI. CONCLUSION

A fast evaluation strategy for substrate parasitics in integrated circuits was presented. A preprocessed, polynomial-based boundary element method was described that is both fast and accurate and allows the real-time extraction process to be completely technology independent. An accelerated BEM matrix solution technique that dramatically reduces the complexity of the extraction process was also presented. The algorithms have been incorporated into a substrate extraction program, SUBTRACT. The extraction tool was shown to be viable in mixed-signal IC design and verification through its deployment in determining substrate parasitics in a mixed-signal video A/D converter IC.

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REFERENCES

[1] T.J. Schmerbeck, R. A. Richetta and L.D. Smith, “A 27 MHz mixed A/D magnetic recording DSP using partial response signalling with maximum likelihood detection,” *Tech. Dig. ISSCC*, pp. 136-137, Feb. ‘91

[2] D.K. Su, M.J. Loinaz, S. Masui and B.A. Wooley,” Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits,” *IEEE JSSC*, vol. 28, no. 4, pp. 420-430, Apr. ‘93.

[3] T.A. Johnson, R.W. Knepper, V. Marcello and W. Wang,” Chip Substrate Resistance Technique for Integrated Circuit Design,” *IEEE Trans. on CAD*, vol. CAD-3, no. 2, pp. 126-134, Apr. ‘84.

[4] N.K. Verghese, D.J. Allstot and S. Masui, “Rapid Simulation of Substrate Coupling Effects in Mixed-Mode ICs,” *Proc. CICC*, May ‘93

[5] F. Clement, E. Zysman, M. Kayal, and M. Declercq, “LAYIN: Toward a Global Solution for Parasitic Coupling Modeling and Visualization,” *Proc. CICC*, pp. 537-540, May ‘94.

[6] T. Smedes, N. P. van der Meijs and A.J. van Genderen, “Boundary element methods for capacitance and substrate resistance calculations in a VLSI layout verification package,” *Proc. International Conf. on Software for Elect. Engg. Analysis and Design*, pp. 337-344, July ‘93.

[7] R. Gharpurey and R.G. Meyer, “Modeling and Analysis of Substrate Coupling in Integrated Circuits,” *Proceedings of the Custom Integrated Circuits Conference*, pp. 7.3.1-7.3.4, May ’95.

[8] Y. Saad and H.M. Schultz, “GMRES: A generalized minimum residual algorithm for solving nonsymmetric linear systems,” *SIAM Journal on Sci. and Stat.Comp.*, vol. 7, no. 3, pp. 856-869, July ‘86.

[9] V. Rokhlin, “Rapid solution of integration equations of classical potential theory,” *Journal of Computational Physics*, vol. 60, no. 2, pp. 187-207, Sept. ‘85.

[10] L. Greengard, *The Rapid Evaluation of Potential Fields in Particle Systems*, M.I.T. Press, Cambridge, Massachusetts, 1988.

[11] K. Nabors and J. White, “FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program,” *IEEE Transactions on CAD*, vol. 10, no. 11, pp. 1147-1459, Nov. ‘91.

[12] N.K. Verghese, *Extraction and Simulation Techniques for Substrate-Coupled Noise in Mixed-Signal Integrated Circuits*, Ph.D. dissertation, Carnegie Mellon University, Aug. ‘95.

[13] N.K. Verghese, D.J. Allstot and M.A. Wolfe, “Fast Parasitic Extraction for Substrate Coupling in Mixed-Signal ICs,” *Proceedings of the Custom Integrated Circuits Conference*, pp. 7.2.1 - 7.2.4, May ‘95.

[14] *TVP 5700 - Triple 8-bit Video Analog-to-Digital Converter*, Product Preview, Texas Instruments Inc., Apr. ‘94.