A High-Level Design and Optimization Tool for Analog RF Receiver Front-Ends

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Abstract

This paper presents a high-level analysis and optimization tool for the design of analog RF receiver front-ends, which takes all design parameters and all aspects of performance degradation (noise, distortion, self-mixing...) into account. The simulations are performed in the spectral domain with a behavioral model library for the RF building blocks. The tool allows to explore alternative RF receiver topologies as well as to investigate design trade-offs within each topology. By having integrated the performance analysis routine within a simulated annealing optimization loop, the tool can also perform an optimal high-level synthesis of a given topology towards a specific application. It then determines the optimal specifications for the RF building blocks such that the required receiver signal quality is met while the overall power and/or area consumption is minimized.

1. Introduction

The market of wireless applications is booming nowadays. The use of digital signal processing and digital signal control has enabled wireless communications with low transmission bit-error rates. Equally important however are the analog transceiver front-ends [1]. The design of RF front-ends was until now always a very intensive process, based on the knowledge and skills of experienced RF designers. But now, the market situation is changing rapidly. The number of wireless applications is growing at a very fast pace and, as time-to-market becomes highly important, this requires the implementation on ever shorter terms of circuits operating at higher frequencies, with higher degrees of integration, lower operating voltages and lower power consumption. In addition, the optimization of each individual building block alone no longer suffices to meet the specifications. Instead, new RF transceiver topologies have to be explored and optimized at the architectural level, before designing the individual building blocks. A design tool which allows such explorations and the fast evaluation of high-level trade-offs in analog RF transceiver design is, however, not yet available today.

This paper presents a high-level design and optimization methodology for analog RF receiver front-ends. This methodology has been implemented as the ORCA (Optimizer for ReCeiver Architectures) prototype tool. Whereas transmitters deal with a well known signal and are therefore relatively straightforward to design, this is not the case with receiver design. Receivers have to handle a highly random and variable antenna signal of which the wanted signal is only a small part. An optimal receiver design is therefore highly dependent on the application, the used topology and the performance of the different types of building blocks used in this topology. The design methodology presented in this paper takes all these aspects into account and allows to evaluate the performance of an RF receiver topology as well as to automatically translate high-level system specifications into a set of specifications for each building block in the topology such that the overall power and/or area consumption of the receiver is minimized.

In section 2, the systematic modeling and analysis methodology for RF receiver topologies is introduced, including effects such as noise, distortion and aliasing. Next, section 3 describes the performance simulation method which operates on signal spectra in the frequency domain, and the optimization loop built around the simulator that allows automatic high-level synthesis of a receiver topology. Section 4 then presents experimental results. Conclusions are provided in section 5.

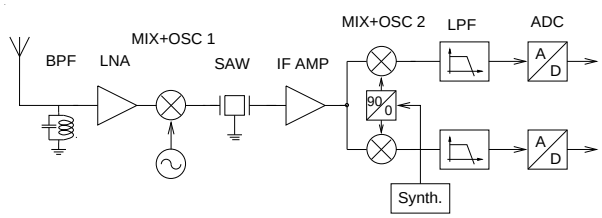

Fig. 1. A combined IF zero-IF receiver topology.

2. RF receiver front-end design

2.1. Receiver performance modeling

Fig. 1 shows an example of an RF receiver topology, a combination of an IF and a zero-IF receiver [2,3]. In successive filtering, amplification and downconversion stages the unwanted neighbor signals are further and further suppressed and the wanted signal is brought down to lower and lower frequencies until the final, low-dynamic-range, low-frequency signal can be sampled with a fairly simple A/D converter. Trade-offs have to be made

in the receiver design, because it is not possible to do all the filtering and downconversion in one stage.

The performance of a receiver is defined as the output SUSR (Signal to Unwanted Signal Ratio) which is the ratio between the power of the undemodulated wanted signal at the output (after the A/D converter) and the total power of all the unwanted signals that are located at the same frequencies as the wanted signal. The unwanted signals can be subdivided in three categories :

- NOISE : all signals generated in a building block that are not correlated to any other signal (thermal noise, shot noise, but also DC offset voltages...).
- DISTORTION : all signals related to (a power of) the input signal (main sources are second- and third-order harmonic distortion and intermodulation, but also self-mixing products).
- ALIASING : all frequency-translated versions of the input signal that did not undergo the wanted frequency translation (e.g. aliasing components in A/D converters, mirror signals in downconverters, phase noise, etc.).

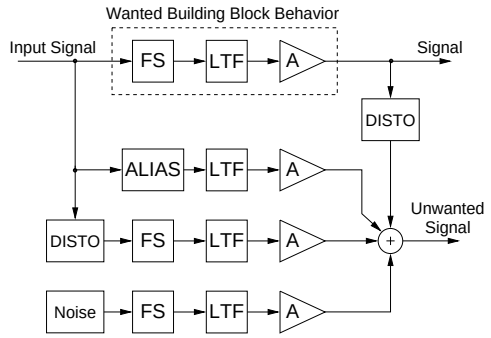

Fig. 2. The processing of wanted and unwanted signals in a building block.

As shown in Fig. 2, the signal processing operations of a receiver building block are completely defined by specifying on one hand the wanted frequency translation (FS) and linear transfer function (the filter characteristic LTF and amplification A) and on the other hand the noise sources (NOISE), the distortion levels (DISTO) and the unwanted frequency translations (ALIAS). Each block thus generates 4 different types of output signals from 1 input signal, which are also handled separately in the RF performance simulations. Distortion is modelled on both the input and the output signal.

Most properties, like self-mixing, aliasing components and the shape of the transfer function, depend on the type of the building block and the chosen IC implementation method. Only a limited number of parameters can be varied freely between certain boundaries during design. Each building block has the following set of parameters :

- $\mathrm{BW_i}$: the bandwidth of the linear transfer function.
- A_i : the overall amplification in the block's passband.
- DR_i : the noise level expressed via the dynamic range
- F_i : the operating frequency (center frequency for filters, local oscillator frequency for mixers).

Only this set of building block specifications is relevant for the trade-offs in receiver design, and are therefore the variables that can be entered by a designer or that are optimized during an optimization run. The power and/or area consumption and the unwanted signal behavior of each building block will have to be modelled as a function of this parameter set.

2.2. Input conditions

The optimization results for a given topology depend highly on the possible input signal conditions, which are represented as a set of power spectral densities S_{0j}, each representing an input situation type that can occur for a certain application, and the signal to unwanted signal ratio $\mathrm{SUSR_j}$ required for each situation. The distribution of the amplification and filtering over the different stages highly depends on these input spectra and the required $SUSR_j$. Preventing saturation for the worst condition, the relationship between the dynamic ranges and bandwidths of two consecutive stages $\mathrm{i-1}$ and i can be determined :

$$\mathrm{DR_i} = \mathrm{DR_{i-1}} \cdot \frac{1}{\mathrm{A_i^2}} \cdot \frac{\mathrm{BW_{i-1}}}{\mathrm{BW_i}} \qquad (1)$$

A higher dynamic range is equivalent to lower noise levels and this can only be realized at the cost of a higher power and area consumption. It is thus important to find, for a given set of input conditions and a desired $SUSR_j$ for each condition, a set of bandwidths BW_i, gains A_i and center frequencies F_i which give the minimal power and/or area consumption.

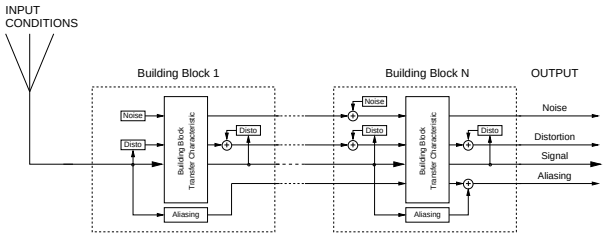

Fig. 3. Signal flow in the performance simulation algorithm.

3. The simulation and optimization method

3.1. Simulation method

Fig. 3 shows the flow diagram of the implemented performance simulator for receiver architectures. Each building block converts, as shown in Fig. 2, an input signal $S_{(i-1)j}$ into an output signal S_{ij} via a frequency translation, a filter operation and an amplification. The unwanted noise, distortion and aliasing signals, however, are processed separately in our simulator in parallel to the wanted signal. It is only after the simulation, at the output of the receiver, that they are combined into the $SUSR_j$ over the wanted output signal's passband. In this way, all contributions can be monitored separately on each intermediate node. Also, nonideal operations on the unwanted signals generated in previous building blocks can be omitted since this would only result in small

higher-order corrections.

The simulator has to keep track of :

- the power spectral density distribution at each node and the signal transfer between the different receiver nodes
- the frequency shifting and aliasing effects
- the distortion and intermodulation effects

Classical SPICE AC analysis cannot be used for this purpose. Transient analysis could theoretically be used. A data sequence, similar to a sampled version of the actual antenna signal, could be applied at the input and the power spectral density distribution on each node could be determined by taking the FFT of the time domain signals. However, this would require impractically large sets of data points, resulting in massive memory and CPU time consumption. Indeed, the signal spectra range from DC to several GHz. The resolution has to be about 1 kHz, since the wanted signal is only a very small part (a few hundred kHz) of the total power spectrum. A data point representation of the signal would then require more than 1 million points. Another problem is how to discriminate between the wanted and the unwanted (noise, distortion, aliasing) signals in the resulting output spectrum.

The harmonic balance simulation technique [4] allows to get a good insight in the different types of nonlinear behavior in RF circuits. The effects of distortion and aliasing can be observed quite accurately, but it is not practical to evaluate with this technique the actual overall performance reduction due to these effects. This would again require the use of more than 1 million data points (now in the frequency domain).

Important for the simulator is thus the representation of the signal spectra. In our approach, the power spectral density distributions S_{ij} are represented symbolically as a sum of bandlimited rational polynomials RP :

$$S_{ij}(f) = \sum \left(\frac{n_0 + n_1 f + n_2 f^2 + \mathrm{K} + n_k f^k}{d_0 + d_1 f + d_2 f^2 + \mathrm{K} + d_l f^l} \Bigg|_{f_{begin}}^{f_{end}} \right) = \sum RP \tag{2}$$

This representation technique gives a high flexibility and a very low memory consumption compared to a data point representation. Most power spectral density shapes in practice are of this form and those which are not can be represented by fitting the actual shape in small intervals to limited-order rational polynomials.

All operations on these signals are implemented as formula manipulations which is easy and fast. For example, filtering is multiplying rational polynomials with rational polynominals, resulting again in a rational polynomial :

$$LTF\left(S_{ij}(f)\right) = \left(\frac{a_0 + a_1 f + \mathrm{K} + a_k f^k}{b_0 + b_1 f + \mathrm{K} + b_l f^l} \right) \cdot \sum \left(\frac{n_0 + n_1 f + n_2 f^2 + \mathrm{K} + n_k f^k}{d_0 + d_1 f + d_2 f^2 + \mathrm{K} + d_l f^l} \Bigg|_{f_{begin}}^{f_{end}} \right) = \sum RP \tag{3}$$

while a frequency translation is obtained by replacing f with $f - F_i$ and calculating the new coefficients :

$$\mathrm{FT}\left(\mathrm{S_{ij}(f)}\right) = \Sigma \left(\frac{\mathrm{n_0 + n_1(f - F_i) + n_2(f - F_i)^2 + K + n_k(f - F_i)^k}}{\mathrm{d_0 + d_1(f - F_i) + d_2(f - F_i)^2 + K + d_l(f - F_i)^1}} \Bigg|_{\mathrm{f_{begin} - F_i}}^{\mathrm{f_{end} - F_i}} \right) = \sum \mathrm{RP} \tag{4}$$

By taking into account both the even and odd terms in the power spectral density representation (2), quadrature signals and quadrature operations can also be handled correctly. The noise power spectra $N_i(f)$ and the unwanted aliasing spectra $AL_{ij}(f)$ can also be represented with formula (2). The distortion spectrum $D_{ij}(f)$ on the other hand is stored as a sum of two or more convolved rational polynomials, which only has to be evaluated at the output of the receiver in a small passband (the bandwidth of the wanted signal).

3.2. Optimization method

The above simulation technique has been integrated within an overall optimization loop, as shown in Fig. 4. This optimization tool determines the optimal set of building block specifications (A_i, BW_i, DR_i, F_i) such that the overall receiver satisfies the required $SUSR_j$ for all input conditions at the smallest overall power and/or area consumption. The performance of the given topology for the specified input condition set is evaluated at each iteration for a different set of building block specifications with the simulator discussed in the previous section.

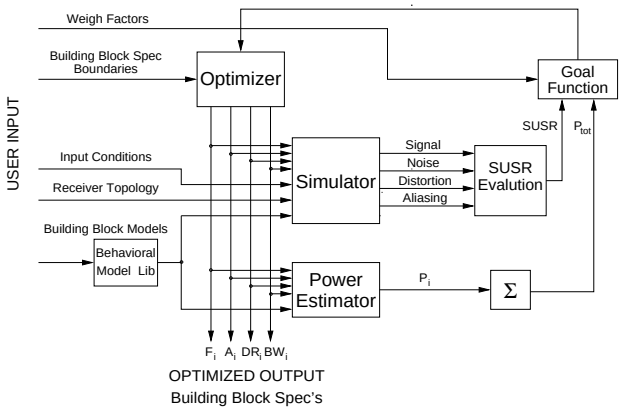

Fig. 4. The ORCA simulation and optimization tool.

A behavioral model library contains high-level models for the different types of receiver building blocks. The models contain the wanted and unwanted (noise, aliasing, distortion) signal operations of each block, and the relationships between the block's specifications and the corresponding power and area consumption. For example, a quite general model for the power consumption $\mathrm{P_i}$ of a block with specifications $\mathrm{A_i}$, $\mathrm{BW_i}$, $\mathrm{DR_i}$ is given by :

$$\mathrm{P_i} = \frac{\mathrm{DR_i} \cdot \mathrm{A_i^2} \cdot \mathrm{BW_i} \cdot \mathrm{kT}}{\eta_i} \tag{5}$$

where the power efficiency η_i is the ratio between the theoretical and actual power needed to obtain these specifications. η_i depends on the building block type, the IC implementation technique and on some of the specifications of the building block. The power efficiency has been calculated for a large number of real-life building

blocks in the library.

The optimization itself is performed by means of a simulated annealing algorithm. Optimization boundaries and weight factors are initially set by the behavioral models and the algorithm, but they can be changed interactively by the user, allowing full control over the design and optimization process.

4. Experimental results

The methodology described in the previous sections has been prototyped in the ORCA (Optimizer for ReCeiver Architectures) tool. ORCA can be used interactively, as a simulator and exploration tool, or as an automatic optimization tool. Results of both cases will be presented. For all the examples in this section the combined IF zero-IF topology of Fig. 1 was used.

When ORCA is used as a simulator, all building block specifications (BW_i, A_i, ...) have to be provided by the user. In this mode the RF designer can quickly compare different topologies or evaluate the influence of different building block specifications on the overall performance of the receiver. Simulation times range from less than 1 minute to several minutes (on a SUN Sparc10) depending on the number of different input conditions that are specified by the user. A typical output of a simulation run is shown in Fig. 5.

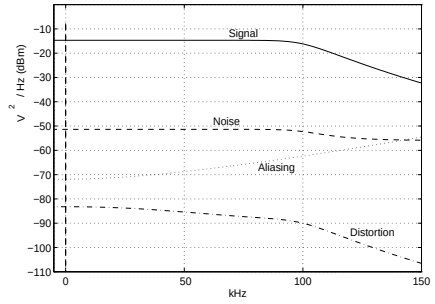

Fig. 5. A typical ORCA simulation result.

The signal band of interest is 100 kHz. The frequency distribution of the wanted and the different unwanted signals (noise, aliased signals and distortion) are displayed separately. Notice the large noise peak at DC due to LO to RF crosstalk in the second mixer, which is typical for zero-IF topologies.

ORCA can also be used in automatic mode, as an optimization tool. In that case the RF designer has to specify the optimization variables (the building block specifications that have to be varied during optimization, e.g. the BW of the bandpass filter BPF), the boundaries for each optimization variable (e.g. 20 - 800 MHz for BW_{BPF}) and the cost function (a weighted sum of the total power consumption and the deviation from the SUSR specification). Due to the nature of simulated annealing, one optimization run will typically take several hours.

Table 1 shows the results obtained from an ORCA optimization run for a specified SUSR of 40 dB. The total power required by the receiver was 50 mW. All italic numbers are optimization results. Finally, Fig. 6 shows the minimal power versus SUSR obtained from several optimization runs with different SUSR specifications.

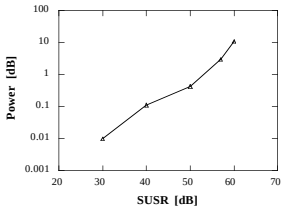

Fig. 6. Optimimal power consumption versus SUSR .

T_i	F_i [MHz]	BW_i [MHz]	A_i [dB]	DR_i [dB]	P_i [mW]
BPF	910.0	*54.0*	0.0	∞	0.0
LNA	0.0	*2680.0*	*28.0*	*50.0*	*30.5*
MIX 1	*793.0*	*1738.0*	*3.4*	*55.0*	*14.5*
SAW	*117.0*	*55.0*	0.0	∞	*0.0013*
IF AMP	0.0	*410.0*	*14.0*	*53.0*	*2.8*
MIX 2	*117.0*	*384.0*	*14.0*	*45.0*	*1.1*
LPF	0.0	*1.23*	*1.2*	*74.0*	*0.126*
ADC	0.0	*8.61*	0.0	*65.0*	*0.216*

Table 1. ORCA optimization results for a SUSR of 40 dB.

5. Conclusions

A methodology for the high-level analysis and optimization of analog RF receiver front-ends has been presented, which allows to explore alternative RF receiver topologies as well as to investigate design trade-offs within each topology. The simulation method separately determines the wanted and all unwanted signals (noise, distortion, aliasing) and all operations are performed in the spectral domain. A built-in optimization loop allows the tool to automatically perform high-level synthesis of RF receivers by translating application-specific system-level specifications, such as the antenna signal spectra and the required output signal quality, into optimum specifications for each building block which minimize the overall power and/or area consumption. Experimental results have been presented that show the practical usefulness of the tool.

References

[1] J. Sevenhans et al., "An analog radio front-end chip set for a 1.9 GHz mobile radio telephone application," *proc. ISSCC*, pp.44-45, Feb. 1994.

[2] C. Marshall et al., "A 2.7V GSM transceiver ICs with on-chip filtering," *proc. ISSCC*, pp.148-149, Feb. 1995.

[3] T. Stetzler et al., "A 2.7V to 4.5V single-chip GSM transceiver RF integrated circuit," *proc. ISSCC*, pp.150-151, Feb. 1995.

[4] K. Kundert, A. Sangiovanni-Vincentelli, "Simulation of nonlinear circuits in the frequency domain," *IEEE Trans. on Computer-Aided Design*, Vol. 5, No. 4, pp. 521-535, Oct. 1986.