Metrics, Techniques and Recent Developments in Mixed-Signal Testing

Gordon W. Roberts
Microelectronics and Computer Systems Laboratory
McGill University
Montreal, CANADA H3A 2A7
Tel: 514-398-6029 Fax: 514-398-4470
http://www.macs.ee.mcgill.ca/~roberts/

Abstract

This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on product cost and quality. We will look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we will argue that analog circuits require very different test methods than those presently used to test digital circuits. We will then describe four common analog test methods and their measurement setups. We will also describe how analog testing can be accomplished using digital sampling techniques. Finally, we shall close this tutorial with a brief description of several developments presently underway on the design of testable mixed-signal circuits.

1. Introduction

With the growing importance of analog circuits in commercial mixed-signal ICs and systems, combined with the demand for shorter design and manufacturing cycles, the need for economical, fast and accurate test methods is readily apparent. At present, mixed-signal ICs are tested using *ad hoc* or unstructured test methods on a wide assortment of expensive analog and digital test equipment. Moreover, test of the analog portion of the mixed-signal circuit is usually considered as an afterthought of design, eliminating any influence that the test engineer may have over the test process, e.g., access to a particular node. In contrast, digital circuits are designed using methodologies that consider up front during the design phase how the circuit will be tested and interfaced to the test equipment. The advantage of such an approach is that the best compromise between functionality, performance, and test can be established, as test requirements become another design constraint. Furthermore, by standardizing the components of the test apparatus, possible test solutions can be incorporated into existing CAD tools to aid the designer in finding the optimum design.

While mixed-signal designs can benefit from similar design and test methodologies, none seems to be prevalent at this time. This stems largely from the nature of an analog circuit, its purpose, and how manufacturing errors influence their desired behavior. It is therefore the intent of this tutorial paper to describe the underlying reason for the difference between analog and digital test, followed by the metrics used to judge an analog or mixed-signal device, and their typical test set-ups. Subsequently, this paper will go on to describe some of the more recent developments presently underway in various research laboratories, including fault analysis, IEEE the proposed IEEE 1149.4 mixed-signal test bus, and methods for built-in self test.

2. The role of test

Consumers today demand high performance and quality in any of the electronic components that they may buy. Low prices and years of problem-free operation with minimal maintenance are now the norm. In order for manufacturers to deliver such products, an extensive testing program must be in place [1], [2]. This is to ensure that only good products are delivered to the consumer and that bad parts are either sent for repair or discarded. Distributing the testing throughout each stage of manufacture (i.e., at wafer, die, board and system assembly) will minimize the cost incurred by testing [3]. A commonly mentioned rule of thumb of test is the *rule of ten* which suggests that the cost of detecting a bad component in a manufactured part increases tenfold at each level of assembly. Thus, discovering its presence early is most desirable.

The question that emerges at this point is what kind of test should be performed, after all, testing does consume resources and takes time to perform. The answer lies with the observation that design errors are unrelated to those caused by manufacturing. Thus, the tests required

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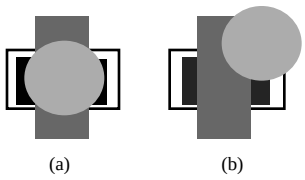

Figure 1: A spot defect creating (a) catastrophic and (b) parametric failure modes in an MOS transistor.

to determine whether a design is acceptable can be very different from those required to determine whether the design has been manufactured correctly. The same is true for analog circuits. However, as we shall describe next, the effects of manufacturing errors on analog circuits are quite different than those which occur with digital circuits. Thus, requiring very different test techniques.

3. Manufacturing defects

In this work we refer to manufacturing errors, or what is commonly referred to as a defects, as any error that leads to a device failure that is caused during the manufacturing phase. There are generally two types of manufacturing defects: those caused by spot or bridging defects, or what we shall refer to as environmental defects, and those caused by process variations. One example of a spot defect is a piece of dust or debris landing on the surface of a wafer of an integrated circuit during its fabrication. The result can then have two different effects classified as catastrophic or parametric. A catastrophic failure is one in which the component is destroyed or uncontrollable. For example, the gate of a transistor is completely removed from the channel region of the transistor by a spot defect as shown in Figure 1(a). A parametric failure, on the other hand, is one in which the component appears to function but may not be within the desired tolerance limits. A transistor that may turn on and off but carries less current than normal is one example.

Component Type	Absolute Tolerance	Matching Tolerance
NPN transistor:		
β	±20%	±5%
V_{BE}	±20 mV	±1 mV
NMOS transistor:		
V_T	±100 mV	±10 mV
k_p	±20%	±1%
Capacitor:		
MOS	±20%	±0.1% - ±1%
poly-poly	±20%	±0.1% - ±1%
Resistor:		
p-type diffused	±20%	±1%
epitaxial	±20%	±5%

Table 1: Absolute value and mismatch tolerances.

This situation may arise by a spot defect removing only a portion of the gate as illustrated in Figure 1(b).

Process variation is generally the result of equipment fluctuations in alignment and performance. In IC manufacturing it leads to an uneven layer deposition across the surface of the wafer. On account of their independent effects on electronic circuits in general, process variation are categorized into two types: global and local. Global variation refers to the systematic variation of a parameter that occurs between the extremities of the device, e.g. transistor threshold voltage may vary systematically from one side of the die to the other. Local variation refers to the small ($< 1\ \mu m^2$) random differences that occur between physically adjacent components. Using the IC example given previously, local variation gives rise to the mismatch error between two physically adjacent transistors. It is interesting to note that no two transistors, resistors, capacitors, etc., will have the same behavior; mismatch will always be present. Device mismatches are one of the fundamental performance limitations in analog circuits, as well as a major reason behind the difficulty encountered with mixed-signal testing. To shed some light on the magnitude of expected process tolerances, we provide in Table 1 a list of absolute value and matching tolerances for several standard IC components. As is evident, the effects of global variations on device behavior is much larger than that experienced by any local variation.

3.1 Impact of defects on digital circuits

To observe the effects that manufacturing defects have on digital circuits, let us consider the CMOS inverter circuit shown in Figure 2(a). Assume that the NMOS and PMOS devices have current gain factors, k_n and k_p, respectively, resulting in the DC transfer characteristic shown in Figure 2(b). Furthermore, let us assume that its pulse response is that shown in Figure 2(c). Hand analysis [4] reveals that the DC transfer characteristic depends on the ratio of k_n to k_p and not on any single current gain factor. So, provided the two transistors are physically close to one another, their current gains will be similar, differing by some small mismatch error. The result is a slight change in the DC transfer characteristic, but nothing very significant. As long as the input signals are within their intended range, the logic function of the inverter circuit will remain the same. The logic function of the inverter is therefore unchanged by the presence of the defect. In contrast, the rise and fall times of the inverter's pulse response is directly dependent on the absolute value of the current gain factors. Thus, to maintain the same logic function, it is important that the current gain factors are large enough to drive the logic level from one state to the next in the time required, i.e. clock period. Digital IC manufacturing ensures that this is achieved by testing the current gains of a small sampling of transistors at various locations on the wafer. If any device fails to meet the required current gain levels, the entire wafer is thrown out.

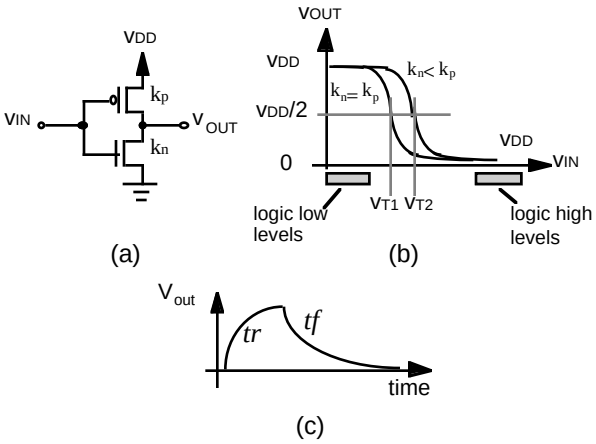

Figure 2: CMOS inverter circuit.

The effect of an environmental defect on a digital circuit is random. A dust particle knocking out the gate of a transistor will cause the logic function of the inverter to change. However, if it only removes a portion of the gate, the inverter may continue to perform the desired logic function as if no defect was present. This is a unique self-correcting property and one that analog circuits do not possess. The bulk of the testing performed on digital circuits is to identify those circuits whose logic function is altered by the presence of an environmental defect.

3.2 Impact of defects on analog circuits

Unlike digital circuits, the function of an analog circuit is sensitive to device mismatches. Analog circuits are also affected by other manufacturing defects, but in ways that are very similar to that described for digital circuits. To illustrate the dependence on device mismatches, consider the op amp inverter circuit shown in Figure 3(a). Assuming an ideal op amp, straightforward circuit analysis reveals that its gain is equal to $-R_2/R_1$. So, with equal resistors, the gain of the amplifier is expected to be -1 V/V. Unfortunately, due to local process variations, R_1 and R_2 will differ. Thus, the gain of the amplifier will not be equal to -1 V/V, but instead, it may equal, say -1.1 V/V. Moreover, repeating the same design at different locations on the same die will be subject to similar effects, however, not identical ones. That is, the gain of each amplifier may become, say -0.91, -0.94, or -1.05 V/V. In essence, the effects of local process variations on each resistor pair results in a level of uncertainty in the actual gain that can be achieved, see Figure 3(b). The same can be said for the function of any analog circuit, thus the expected level of uncertainty is an important design parameter, and not one that is left for chance. So, from a test point-of-view, it is meaningless to talk about measuring a function without assigning a range of acceptability. Table 2 summarizes the effect that various manufacturing defects have on the behavior of both digital and analog circuits.

The astute reader may be wondering why one does not directly measure the mismatch error in the circuit, and avoid the complexity associated with measuring the circuit's function. After all, this approach worked quite well for digital circuits. The answer to this question has two parts. Firstly, there is no obvious way in which to measure all the mismatch errors present in a circuit and, secondly, mismatch errors do not necessarily add to create a larger error; it is possible for errors to cancel. As an example, a circuit that realizes a gain of 1 V/V ± 5% can be constructed from a cascade of two op amp inverter circuits having a nominal gain of -1 V/V. If one of the inverter circuits has an actual gain of -0.7 V/V and the other -1.4 V/V then their combined gains would be 0.98 V/V, or an error of less than -2%. Clearly, on an individual basis, each stage when compared against the 5% tolerance band would be considered unacceptable. Test decisions based directly on measurements of individual component variations lead to an unacceptable number of good parts being rejected (i.e., false alarms) resulting in reduced yields.

Conversely, the acceptability of the system should not be determined from a test that is based on the performance of several analog circuits whose normal behaviors are independent of one another. This stems from the fact that a substantial number of defective parts can appear acceptable during the test, as errors in different circuits can mask one another. For example, a test decision based on, say, the power supply current (I_{DDQ}) of a mixed-signal device consisting of an acceptable A/D and D/A converter and a defective filter circuit can collectively appear as a good part. To minimize the risk, elementary statistical analysis suggests the only way to improve the situation is to reduce the tolerance band around individual components. Of course, this results in an increase in the

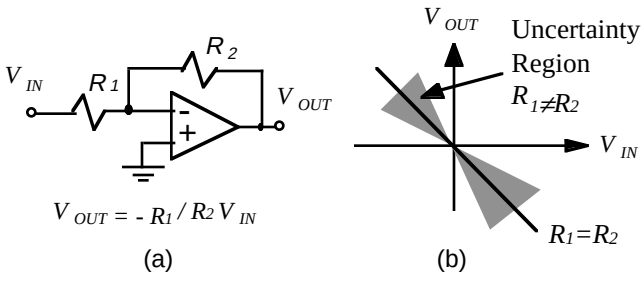

Figure 3: Op amp inverter circuit.

Manufacturing Errors	Impact on Circuit	
	Digital	Analog
Environmental	random	random
Process Variations:		
global	none provide within bound	none provide within bound
local	none	random

Table 2: Effects of manufacturing defects.

cost of the part and is generally frowned upon. Analog and mixed-signal circuits are usually pushing the envelop of technology and it is generally felt that any improvement in the tolerance bands can be used more effectively by improving the performance of the device rather than easing the test requirements. Of course, better understanding of the economic break-even point could better serve the electronics' manufacturer.

The conclusion from the above discussion is that there does not appear to be any easy way out of the mixed-signal test quandary. It appears at this time that the most economical method of testing analog and mixed-signal devices is to test their function directly. If particular catastrophic failures are expected, similar to those described for digital circuits, then a prescreening test may be called for. Here the power supply current monitoring method alluded to above may play a useful role [5]. However, in the end, some form of functional testing is necessary before the part can be accepted. Today, most analog or mixed-signal circuits exist at the interface between the analog world and the digital compute engine, and are intended to have high-performance capabilities. Thus, testing their functionality requires very expensive test equipment, performing lengthy and elaborate test routines. It is therefore not surprising that only a small number of mixed-signal devices are available from commercial electronic vendors when so much effort must be devoted to their quality assurance. Section 7 will consider some possible ways of improving the present situation.

4. Analog circuit functions

Of the many roles that analog circuits play in electronic systems, probably the most important is that in signal processing. In much the same way that a numerical analyst writes a computer program, analog circuit designers configure electronic sub-circuits so that a particular function is realized. They are usually guided by a mathematical description of the function they want, expressed in terms of algebraic, integral, and differential operations. For example, an eighth-order switched-capacitor elliptical filter would be described by an eighth-order difference equation. Similarly, at the core of an algorithmic A/D converter would be a divide-by-two circuit that would be used to aid in the conversion of the floating point (analog) number representation to its binary number equivalent. Owing to the nonlinear behavior of the underlying components, e.g. transistors, only an approximation of the function is actually realized. Through the application of negative feedback, the approximation is improved and made less sensitive to process variations. It is therefore the goal of the circuit designer to obtain the desired function within the acceptable error subject to the underlying process variations. What constitutes acceptable error depends on the application and is impossible to generalize. Thus, every analog circuit is characterized by its own special set of measurements that attempt to quantify this approximation in the environment that it is intended to be used.

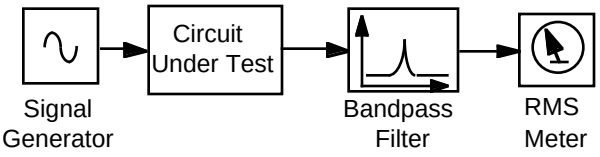

Figure 4: Typical analog test setup.

5. Test set-up and measurements

The most basic analog measurement setup consists of a signal generator exciting the circuit-under-test and an instrument to extract the appropriate parameter from the circuit's output response. Depending on the purpose of the test, the signal generator may be generating a DC, sinusoid, square-wave, or some arbitrary waveform shape. Which signal is used depends on the type of measurement that is to be taken. There are four main measurement categories:

1) *DC measurements*: they measure the static behavior of the circuit such as leakage currents, output resistance, transfer characteristics and offsets.
2) *AC measurements*: they measure both the small- and large-signal frequency response behavior of the circuit. Distortion measurements are also included in this test.
3) *Transient or time-domain measurements*: they measure the behavior of the circuit subject to signal shapes that the circuit will experience in its intended application.
4) *Noise measurements*: they measure the variation in the signal that appears at the circuit's output when the input is set to zero.

A common setup that is able to perform several of the above measurements (1, 2 and 4) is shown in Figure 4. It consists of a sinusoidal signal generator with variable amplitude and frequency control. The output of the circuit-under-test is then filtered by a narrowband bandpass filter. The center frequency of the filter is tunable, and may or may not track the frequency of the input signal. Finally, the power associated with the filtered output signal, once settled, is then measured using a true-RMS power meter. Transient-type measurements are not more complicated, but usually require very specialized equipment to generate and capture the appropriate test signal, e.g., bit-error rate.

Tests involving sinusoidal excitation is probably the most common among linear circuits, such as amplifiers, data converters and filter circuits. Amidst all waveforms, the sinusoid is unique in that its shape is not altered by its transmission through a linear circuit, only its magnitude and phase are changed. In contrast, a non-linear circuit will alter the shape of a sinusoidal input. The more

non-linear the circuit is, the greater the change in the shape of the sinusoid. One means of quantifying the extent of the non-linearity present in a circuit is by observing the power distributed in the frequency components contained in the output signal using a Fourier Analysis. Using the setup shown in Figure 4, this would be obtained by exciting the circuit-under-test using a sinusoid and by measuring the power appearing at the output of the bandpass filter as it is tuned to discrete frequencies across the frequency band of interest. Figure 5 illustrates a typical power spectral density plot obtained using these methods. The fundamental component of the output signal is clearly visible, followed by several harmonics. Also shown in the plot is the noise floor of the circuit-under-test. This floor represents the smallest signal that can be distinguished from the noise generated by the circuit. By comparing the power contained in the harmonics to that in the fundamental signal, a measure of Total Harmonic Distortion (THD) is obtained. By comparing the fundamental power to the noise power over a specified bandwidth, one obtains the signal-to-noise ratio (SNR). By altering the frequency and amplitude of the input sinusoidal signal, or by adding an additional tone with the input signal, other transmission parameters can be derived from the power spectral density plot [6].

6. DSP-Based Testing

Since the early eighties, digital signal processing (DSP) has altered the traditional test setup shown in Figure 4 to that shown in Figure 6. Through the application of analog-to-digital (A/D) and analog-to-digital (D/A) data converters, and a very fast compute engine for performing vector manipulations, the function of each analog instrument can be emulated by a software program [7], [8].

The basic idea behind the DSP-based test station is that a signal, possibly sinusoidal, is numerically computed by the digital compute engine and then applied to the D/A block for conversion into analog form. The resulting analog signal is then applied to the circuit-under-test from which its response is digitized by the A/D converter and passed on to the digital compute engine for further processing. Depending on the measurement that is required, the appropriate software would be loaded in place.

The first obvious advantage that comes from this

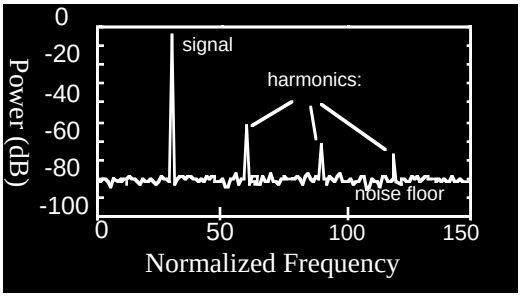

Figure 5: Power spectral density plot.

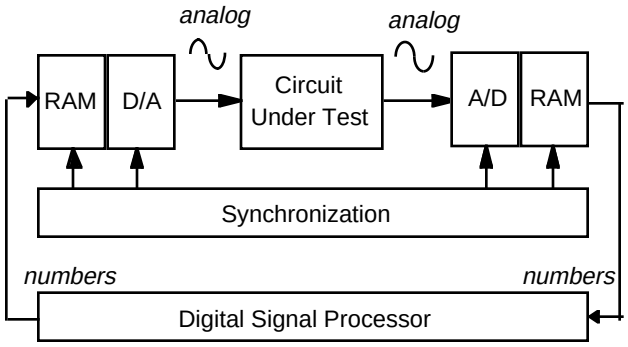

Figure 6: DSP-based measurement system.

approach is the flexibility that programmability provides. The same hardware can be used to perform a multitude of test functions. Secondly, the correction factors associated with a system calibration can be easily incorporated into the routine of any emulated instrument. Thus, correcting for the effects of drift and aging that comes from running test equipment continuously for 24 hours a day, 7 days a week. A less obvious advantage, but equally important, is the ability to pipeline the different phases of the test procedure. On account of the discrete events that are taking place, operations that do not need to run in real-time can be delayed and run in parallel with the operations of the next device. Finally, coherent testing provides a means in which to gather information using the least number of samples. Owing to its importance to DSP-based testing, a brief description is given below.

6.1 Coherent testing

One may be wondering at this point whether digitizing the excitation and response of the circuit-under-test somehow degrades the accuracy of the measurement or loses information. The answer is simply no, as Shannon so succinctly pointed out [9]. His observation suggests that the DSP-based test station has the same amount of information to work with as does the test station shown in Figure 4. More recently, Mahoney [7] pointed out that a DSP-based test station using an *N*-point Fast Fourier Transform (FFT) with rectangular windowing (i.e., no additional post-processing) can perform a much faster and more accurate frequency-selective power measurement than the setup of Figure 4. This is a result of coherent sampling and by eliminating the analog implementation of the squaring operation in the true-RMS power meter. He coined this test arrangement as *coherent testing*. As test time is of primary importance in a production environment, this observation was significant and lead to the creation of a new family of mixed-signal testers. Basically, coherent testing establishes which input test frequencies can be used to perform an accurate sinusoidal test using an *N*-point FFT. According to [8], the test frequency F_T is selected according to the following

$$F_T = \frac{M}{N} F_S , \qquad (1)$$

where F_S is the sampling rate and M represents an arbitrary integer, usually less than $N/2$ and has no factors common with N, i.e., M and N are relatively-prime. The latter ensures that each point is unique in the N-point set, thereby maximizing the information content. An alternative description of the relationship given in Eqn. (1) is that the test frequency should only be selected as a harmonic of F_S/N, the so-called primitive frequency.

6.2 Multi-tone testing

By combining several sinusoids harmonically related to the primitive frequency of the test sequence, a very effective signal for probing the frequency characteristics of a circuit in a single measurement is obtained. Such a signal is known as a multi-tone signal [8]. Multi-tone signals are also very important signals for probing the nonlinear behavior of narrowband circuits, as they provide intermodulation distortion components that lie in-band. Multi-tone signals can also be used to generate a pseudo-random noise signal, by including a fairly broad selection of tones [10]. With independent control over both the amplitude and phase of each tone, energy in the signal can be distributed over time in an optimum manner thereby avoiding a high crest factor.

6.3 RF measurements

Through the application of heterodyning or undersampling, DSP-based test stations can extend their frequency measurement capabilities to the IF or RF frequency bands [11]. The basic idea is to excite a circuit-under-test using an IF or RF signal generated by a frequency synthesizer and translate its response back down into the baseband range of the digitizer for DSP processing. By doing so, most of the advantages of DSP for test are maintained.

6.4 Noise effects

Noise is present in all signals captured by the digitizer. Noise, in general, has many different sources: circuit-generated, static and man-made. We are usually only concerned about circuit noise, as it sets the lower limit of the maximum dynamic range available in a circuit. The influence from the other two sources of noise is minimized through good board layout and power supply decoupling. For the most part, circuit noise creates a randomness in the captured signal, resulting in a different measurement each time the test is run. Thus, noise adds an additional uncertainty with the circuit's function and must be accounted for when selecting the test limits. Statistical theory reveals that the amount of variation in a measurement will decrease inversely with the square-root of the number of samples in the measurement set. However, increasing the number of samples, increases the test time. Therefore a good compromise between acceptable variation and test time must be established. An in-depth discussion of the effects of noise on DSP-based measurements can be found in [12].

7. New test developments

It should be clear from the above discussion that mixed-signal devices will not benefit from the same test advancements that digital circuits presently experience. However, that is not to say that all is lost on the mixed-signal test front. Much can be done and should be done if the cost of mixed-signal testing is to be reduced. As in digital test, most of the mixed-signal research community advocates some form of *design-for-testability* as it is believed that the best compromise between functionality, performance, and test can only be achieved early in the design cycle. It is therefore the purpose of this section to briefly describe the directions and recent results of several advancements in this area.

7.1 Analog fault analysis

An area of research that is gaining some ground in mixed-signal testing is the concept of fault modeling [13] [14]. Fault modeling is a concept that has its roots in digital testing [15]. Fault modeling for analog circuits serves to identify the test conditions that will expose the presence of a fault in a circuit with the least amount of test effort. For catastrophic defects, fault modeling is a very effective way of identifying the optimum test setup. Unfortunately, for parametric failures, it quickly becomes unwieldy due to the amount of simulation time required. For a moderately sized analog circuit, such as a second-order delta-sigma modulator used in data conversion applications, it is not uncommon to run a SPICE simulation continuously for a week on a SUN SPARC 10 workstation before a single measure of the THD is available. With that said, effort is underway attempting to rank-order various tests for popular mixed-signal circuits. By assigning probabilities to potential failure modes, the order of the tests are arranged so that, on average, the least amount of time is spent searching for defective parts [16].

7.2 Circuit schemes for test

With such high levels of integration possible today using submicron VLSI technologies, it is both feasible and beneficial to consider placing all or part of the test circuitry directly on the same die as the desired circuit. Referring back to Figure 4 this would include the test stimulus, parameter extraction or measurement circuitry, and equally important, the interconnect and control circuits. Some of the benefits are: (1) it facilitates design-for-test, (2) provides a hierarchical test solution, as the test circuits can be used at all levels of the system, from the IC-level to the board and system-levels, thereby maximizing the return on the test hardware investment, and (3) standardization which simplifies automation and the integration of test into present day CAD facilities.

The following is a brief description of some of the circuit techniques that have been proposed for making mixed-signal circuits more easily testable. We limit our discussion to those schemes that have been reported to be prototyped or bench tested.

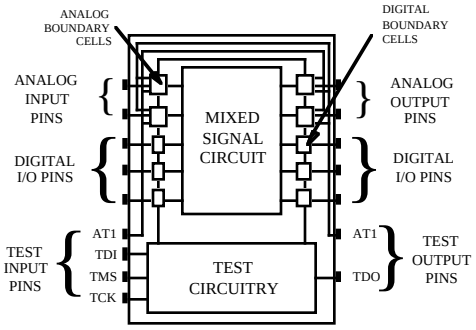

Figure 7: Architecture of IEEE mixed-signal test bus.

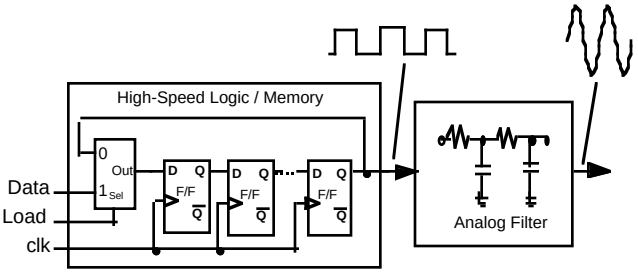

Figure 8: Analog test signal generation using a one-bit digital bit-stream.

Analog test bus

One of the most significant advancements in mixed-signal test is the proposed IEEE P1149.4 mixed-signal test bus standard. Over the past four years a group of international companies and R&D institutions have been working together to define the standard and discuss its compatibility with the IEEE 1149.1 digital test bus standard. The basic idea of the mixed-signal test bus is the inclusion of a set of analog boundary cells and two analog buses connected to two dedicated pins (AT1 and AT2) that allow the analog portions of the mixed-signal device to be tested in much the same manner as with the digital boundary-scan technique [17]. Figure 7 illustrates the basic architecture of the proposed IEEE 1149.4 mixed-signal test bus. Interested readers can learn more about this proposal and its current status by referring to the most recent proceedings of the International Test Conference.

Scan-based signal generation

Very recently a method [18] has been developed which makes use of the memory elements (i.e., flip-flops) in the digital boundary cells of the IEEE 1149.1 test standard to provide storage for a short periodic one-bit sequence that when filtered provides a high-quality analog test stimulus (see Figure 8). For an N-bit sequence being clocked at a rate of F_S, tones harmonically related to the primitive frequency F_S/N are available for excitation in much the same way as that described in Section 6. Similarly, if on-chip RAM is available then it can be used to store and play-back the appropriate bit-pattern. Except for the parameter extraction circuitry, a simple RC filter circuit and some interconnect, the digital boundary scan configuration provides the rest.

Built-in self test

One of the earliest proposal for a fully integrated built-in self-test was that made by a group of AT&T engineers for verifying the monotonicity of an Nyquist-rate A/D converter circuit [19]. An illustration of the proposal is shown in Figure 9. A linear ramp voltage is generated on chip and applied to the input of the A/D converter during test. The output codes are then checked for monotonicity by comparing the present output code with the past code. If true, the output counter is incremented. If false, the test is terminated and a fail flag is set. A counter keeps track of the number of successful comparisons. The final count is then checked against the expected value and a go/no-go type decision is then made. The final count can also be retrieved for possible diagnostics. A straightforward extension is to add additional registers whereby a histogram of the output codes can be obtained over an extended period of test time. The data in this histogram can then be used to determine the linearity of the data converter according to the integral nonlinearity error (INL) and differential linearity error (DLE) type tests.

Another self-test scheme is the so-called MADBIST scheme illustrated in Figure 10. This technique is applicable to devices containing A/D and D/A data converters, and some computing resources [20], although the technique is equally valid for devices containing only A/Ds. The basic idea is that an all-digital on-chip $\Delta\Sigma$ modulation oscillator circuit [21] generates a single-bit digital sequence as the test stimulus for the A/D converter. Within this binary sequence is a well-behaved sinusoid (or multi-tone) and a residual signal whose spectral properties are orthogonal to one another. This signal is then applied to the input of the A/D circuit whose anti-aliasing filter (AAF) suppresses the residual signal and allows the sinusoid to pass unattenuated. The A/D is then excited in the usual way and its output response is then processed using an FFT, if available on-chip, or a narrowband digital filter technique together with a peak detector. A go/no-go type decision is then made. Subsequently, another phase of the test is run whereby the D/A circuit is tested by exciting it with a similar type of digital test signal and whose output is then digitized by the A/D circuit. Once the D/A is

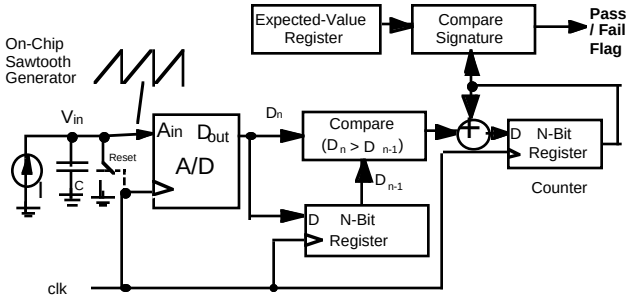

Figure 9: BIST for an A/D converter.

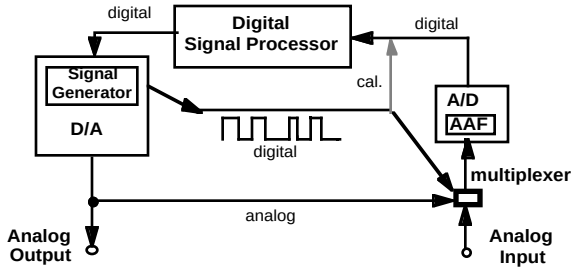

Figure 10: The MADBIST scheme.

considered functional, both data converters can then be used to measure other analog circuits, in much the same way as the DSP-based test setup shown in Figure 6. The latter approach has been proposed as a means of testing bandpass-type mixed-signal devices such as those used in wireless communication systems [22].

Concurrent error detection

Another important research activity is in the area of concurrent error detection for analog and mixed-signal circuits. These techniques are used for detecting the presence of a defect that has manifested itself after the product was tested and sent to the customer for normal operation. A survey paper describing these techniques is provided in [23].

8. Conclusions

The function of an analog circuit is sensitive to local process variations whereas digital circuits are not. At the time of this writing, the most economical way of testing analog and mixed-signal circuits is to measure their function directly. A level of uncertainty caused by local process variations must be accounted for, as well as the uncertainty created by circuit generated noise. It is also important to realize that the function of an analog circuit is only approximately realized, resulting in another level of uncertainty on account of the difficulties in which to track them. This tutorial paper described several common test techniques, with an emphasis on spectral-based measurements using digital sampling techniques. New developments that help to make mixed-signal circuits more testable were also described.

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