DESIGN OF A PROGRAMMABLE TEMPERATURE MONITORING DEVICE FOR TAGGING SMALL FISH

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ABSTRACT

This paper describes the design of an archival temperature monitoring tag to be used to collect habitat information of Atlantic salmon during the marine phase of the species' natural history. The monolithic circuit should not exceed an average power dissipation of 5μW so that a small 3V lithium battery of 50mAh charge will provide the device with the expected lifetime of 3 years. The thermal sensor is realized by a pn-junction. The recorded junction voltages are digitized and stored in static RAM cells. Upon retrieval of the tag, the stored temperature values will be transfered to a computer where the geographical location of the fish at the actual sampling time will be deduced through retrospective navigation based on known sea temperature distribution.

1. INTRODUCTION

This work addresses the need to develop a monolithic circuit that collects physical habitat information, specifically temperature, of individual Atlantic salmon during the marine phase of the species' natural history. Since survival of Atlantic salmon is of great interest to biologists as well as commercial fishermen [1], it is crucially important to learn more about their behavior at sea. By exactly recording water temperature, the unknown geographical location of the fish at the actual sampling time can later, i.e., after the tag's retrieval, be deduced from the stored values through retrospective navigation based on known sea temperature distribution [1], [2].

Young Atlantic salmon swim downstream and enter the sea while the they are still small, viz., 15-20cm total length. Consequently, the archival device must be small enough to not hinder the animal. Low return rates of tagged fish, by reason of expected mortality, dictate that the device also be of low cost so that many fish can be tagged. Finally, since the fishes' sojourn at sea can last 2-3 years, the system's power requirements must be minimized so that the desired lifetime of 3 years can be achieved by employing an inexpensive small battery similar to the ones used in electronic wrist watches. All of the above requirements call for a monolithic implementation of the archival tag.

This paper is organized as follows. Section 2 briefly describes the system configuration and the tag's programmable sampling protocol. The next section addresses the design and the implementation of the low-power oscillator circuit. Section 4 deals with the thermal sensor and presents some preliminary results obtained from first silicon. Section 5, finally, contains some concluding remarks.

2. SYSTEM CONSIDERATIONS

Fig.1 shows a block diagram of the entire system, including the battery and a host PC for programming and data retrieval. In essence, the CMOS chip comprises a local oscillator, a thermal sensor, an A/D converter, a digital memory (static RAM cells) and the necessary control and interface logic.

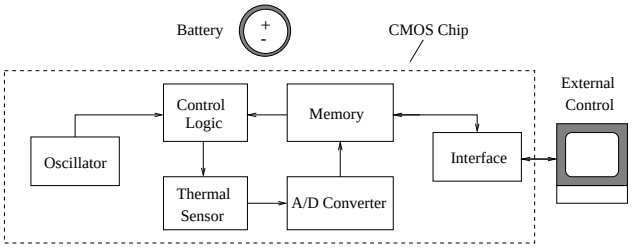

Figure 1. Block diagram of programmable temperature monitoring archival tag.

The chip will be powered by a tiny 3V lithium battery with a maximum charge of 50mAh. Since the device is supposed to remain operational for 3 years, the average current consumed by the monolithic device must be less than $1.9\mu A$. Fortunately, the accumulated time during which the tag actively senses, processes and records the water temperature represents a very small fraction of it's total lifetime. Consequently, most of the chip's circuitry can be turned off during the time in between measurements. The only permanently active blocks will be the digital memory and the timing circuit, i.e., the oscillator and some associated control logic. The power will thus predominantly be consumed by the few permanently active cells, most importantly the oscillator. To illustrate this point, let us assume that the system stays in the active sampling mode for 5 seconds per day. Furthermore, we presume that the power demand dur-

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ing this active phase increases 1,000 fold. Even for such a "busy" scenario, the dynamic power represents less than 6% of the static power dissipation.

The tag possesses a simple serial communication link to the external world (i.e., a host PC). This link consists of five physical lines, 2 for the power supply, 2 for control and one for data. Please note that this interface is activated only twice during the tag's entire lifetime. The first activation, occurring after the insertion of the battery, serves to download a tag ID and specific sampling protocol parameters; the second external data interchange takes place after the tag's successful recovery and serves to retrieve the ID and the recorded temperature values from the chip's memory. In between these two events, the tag's external connections are sealed from the outside world to guarantee integrity of the internal functions. Upon retrieval, the off-chip connective pads of the device must be re-exposed by mechanical or chemical means.

To maximize the versatility of the archival tag, the proposed device must be able to accommodate a variety of different temperature sampling modes. This has been achieved by characterizing the sampling protocol by three variable parameters. They are the episode interval T_e, the sampling interval T_s and the number of samples per episode, n, as illustrated in Fig.2. Note that the episode samples can be averaged so that only a single value needs to be stored in the chip's memory.

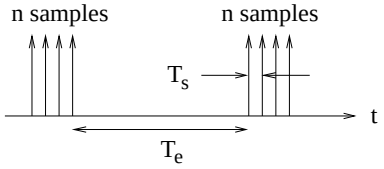

Figure 2. Proposed three parameter sampling protocol.

The above triplet of control parameters is supplemented by a fourth variable, T_a, which defines the device's activation time, i.e., the time that elapses between the initial programming and the sensing of the first temperature value.

The total number of samples taken will be limited by the chip's memory capacity. This quantity is determined by the available chip area. The currently envisioned $1.2\mu m$ CMOS process achieves a memory density of approximately $1kbit/mm^2$. Saving one value per day over 3 years and presuming a resolution of 8 bits per sample thus requires approximately $8mm^2$ of silicon real estate.

3. LOW POWER OSCILLATOR

As previously pointed out, the oscillator most crucially influences the power dissipation of the archival tag. It is therefore of paramount importance to minimize the power demand of this cell.

While most highly accurate electronic time pieces employ crystal oscillators [3], we have opted for an entirely monolithic solution to minimize device size and ultimate fabrication cost. The chosen solution is based on a modified ring oscillator which is driven by a supply independent bias current. The corresponding circuit is depicted in Fig.3. Note that all MOS devices are operated in the sub-threshold region. The core of the circuit is formed by a 15-stage ring oscillator (M_{o1} to M_{o2n}) which is embedded in between the two current mirror devices M_{b5} and M_{b6}, respectively. These two transistors not only control the oscillator current but also limit the output swing of the inverter cascade. In order to achieve a sharp, rail-to-rail square wave output, the oscillator has been complemented by a differential output stage (M_1 to M_9). The square wave output signal drives the input of a binary counter.

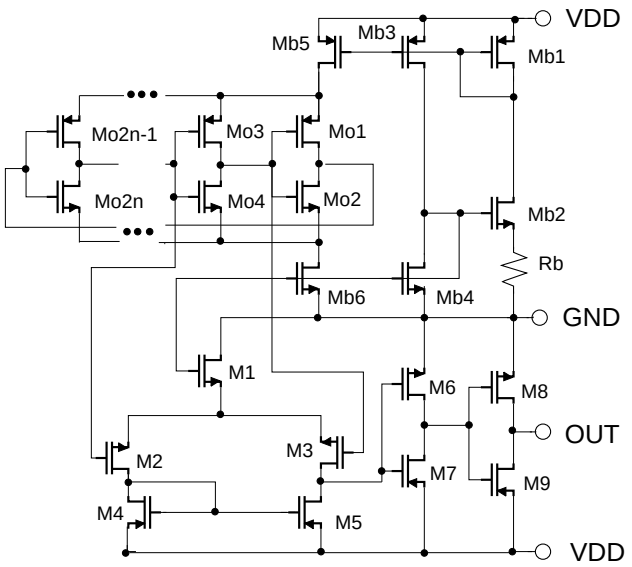

Figure 3. Ring oscillator with constant current source and edge sharpening output stage.

The oscillator circuit has been layed out for a $1.2\mu m$ n-well CMOS process and is currently in fabrication. Fig.4 shows some simulated curves which display the power dissipation and the output frequency as a function of supply voltage and ambient temperature. Note that all simulations have been carried out with layout extracted input files using SPICE level 3 MOS model parameters. According to the depicted results, the circuit is very tolerant with regard to supply voltage variations. Furthermore, at the nominal supply voltage of 3V, the circuit dissipates approximately $1\mu W$ of power, a value that certainly dose not strain the power budget. Unfortunately, the oscillator's output frequency is significantly affected by temperature variations. For example, a temperature change from 0^0C to 20^0C causes the oscillator frequency to increase from 37kHz to 57kHz (V_{DD}=3V).

Since the model parameters for MOS devices operated in the sub-threshold region are not yet well established, practi-

cal values of supply current and output frequency are likely to deviate considerably from their target values. Nevertheless, further silicon prototypes should help to significantly narrow down the remaining interval of uncertainty.

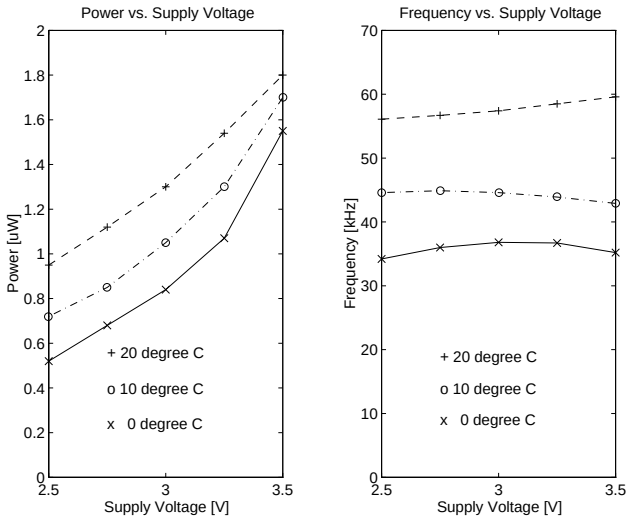

Figure 4. Power dissipation and output frequency of the ring oscillator as a function of supply voltage and ambient temperature.

The in Fig.4 displayed temperature dependence of the supply current and the correspondingly increasing output frequency represent a major drawback of the proposed subthreshold ring oscillator. However, in view of the fact that all temperature variations are well recorded in the tag's memory, it may still remain a viable solution, because the stored temperature values enable a retro-active linearization of the time scale after the data have been recovered. Finally, the remaining thermally induced errors are not expected to significantly affect the post-retrieval retrospective navigation process since the fishes' daily migration patters are relatively small when compared to the large scale of the spacio-temporal map of the North Atlantic.

4. TEMPERATURE SENSOR

The thermal sensor is implemented by a simple pn-junction [4]. This junction (or diode) also forms a vital part of the bandgap reference voltage source which is required for the subsequent A/D conversion process. Since conversion speed is not essential for this application, the A/D cell is implemented by a dual-slope serial converter realized by switched-capacitor techniques.

The CMOS compatible bandgap reference circuit [5] together with an additional voltage follower and a differential output amplifier is shown in Fig.5.

Since the bandgap reference has to accommodate a relatively small temperature range, viz., -4^{0}C to +24^{0}C, and the required resolution of the sensor does not have to be better than 0.5^{0}C, no additional voltage correction scheme is deemed necessary.

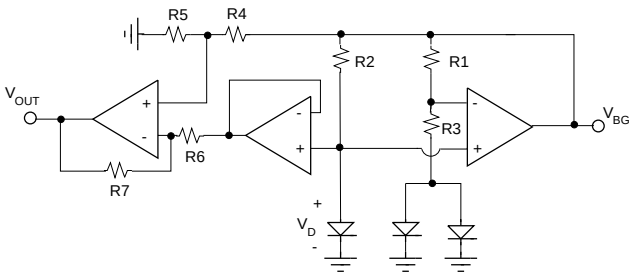

Figure 5. Temperature sensor and bandgap reference circuit with pre-amplifier.

The two governing equations for the bandgap voltage V_{BG} and the differential amplifier output voltage V_{OUT} are

$$V_{BG} = V_D + \frac{R_1}{R_3} V_{TH}\ ln(2) \tag{1}$$

$$V_{OUT} = V_{BG}\frac{R_5(R_6+R_7)}{R_6(R_4+R_5)} - V_D\ \frac{R_7}{R_6} \tag{2}$$

where V_{TH} denotes the thermal voltage while V_D represents the temperature dependent sensor output voltage.

To keep the branch currents of the bandgap reference circuit reasonably small while still allowing an area efficient implementation of the resistors, we have set the two elements R_1 and R_2 equal to 64kΩ. Thermal stability for V_{BG} dictates an R_3 value of 2kΩ (cf. equation. (1)). This yields two equal branch currents for the bandgap reference of approximately $10\mu A$. The resistors of the additional differential amplifier, i.e., the elements R_4, R_5, R_6 and R_7, have been chosen to keep V_{out} within the range from 1V to 2V while establishing similar branch current values.

Fig.6 depicts the layout of the first prototype implementation of the sensor/bandgap reference circuit with the complementary voltage follower and differential output amplifier.

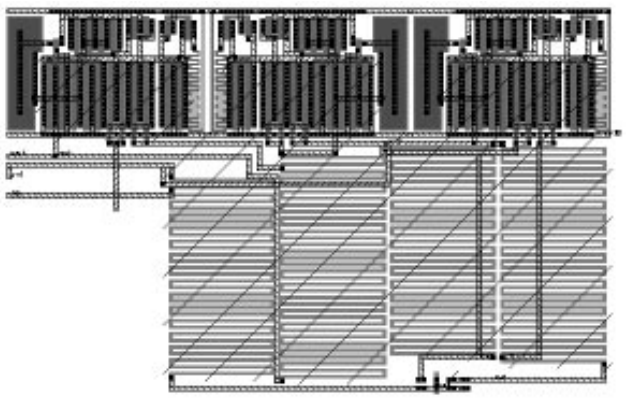

Figure 6. Layout of temperature sensor/bandgap reference circuit and complementary output amplifier.

The three amplifiers (the top row cells in Fig.6) have been realized as conventional two-stage CMOS op-amps with p-

MOS input stages and capacitive phase compensation circuits. The bias currents have been established by supply voltage independent current sources.

Among the available resistive layers, i.e., well, n-diffusion, p-diffusion and polycrystalline silicon, we have chosen to use the p-diffusion layer since it exhibits the highest sheet resistance (approximately 70Ω) and thus yields the most compact resistor implementation. To be able to adjust for process induced deviations of the sensor output voltage V_D as well as the bandgap voltage V_{BG}, the two elements R_4 and R_5 have been realized off chip in the first prototype run.

The three diodes, finally, which are barely visible on the bottom right hand side of Fig.6, have been formed by simple p-diffusion to n-well junctions.

Fig.7 shows some preliminary test results obtained from the first $2\mu m$ implementation of the thermal sensor/bandgap circuit.

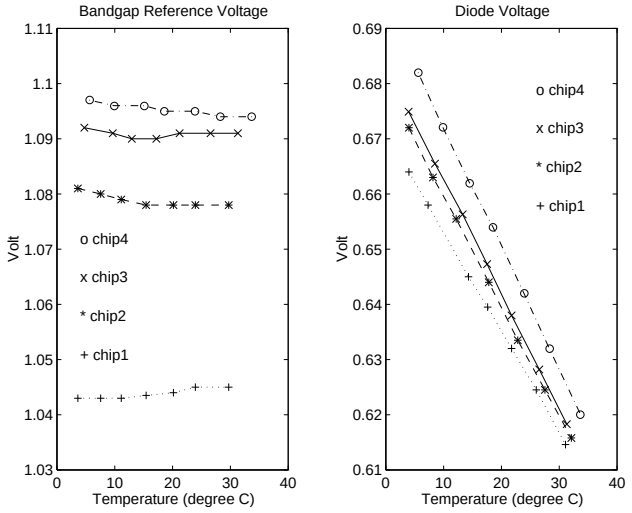

Figure 7. Measured values of bandgap and pn-junction voltages obtained form the first four test chips.

The measurements obtained from the first 4 prototype chips confirm the expected linear relationship between temperature and pn-junction voltage. The maximum variation of the bandgap voltage within the observed temperature interval, i.e., 3^0C to 34^0C, is 3mV. The voltage variation between the different chips, however, is relatively large (54mV in the worst case). By increasing the junction cross section in subsequent fabrication runs, we hope to be able to reduce this chip to chip variance.

To achieve the desired sensor resolution of 0.5^0C over the range of 28^0C, a 6-bit A/D converter would suffice. However, we have opted to employ an 8-bit converter. The excess dynamic range provides enough robustness with regard to gain and offset errors of the sensor output so that the relatively complex thermal calibration procedure can be postponed until after the tag has successfully been recovered. Since only a small fraction of all tags used in a certain study will be returned, this reversal of calibration and retrieval can translate into a significant cost reduction.

5. CONCLUSIONS

We have presented the design and the implementation of a low power all CMOS temperature monitoring device. Apart from the interface circuitry and the sub-threshold ring oscillator, all on-chip system components have been prototyped by a 2μm CMOS process. In order to increase the tag's memory capacity, we are currently re-fabricating the various circuit components by a 1.2μm CMOS process.

The major drawback of the current system is the susceptibility of the timing circuitry to changes of the ambient temperature. For future systems with tighter timing constraints, it may thus become necessary to employ a quartz stable oscillator.

The presented temperature monitoring system is a first version of a monolithic tagging device. Future generations of such devices are expected to become more versatile by also incorporating light and possibly pressure sensing circuitry.

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