Δ-Σ Frequency-to-Time Conversion by Triangularly Weighted ZC Counter

M. Høvin, S. Kiaei and T.S. Lande

Δ-Σ noise-shaping techniques [1] have found extensive use in both A/D and D/A conversion systems. The main reason for their popularity is that many of the Nyquist rate conversion problems are moved from the analogue over to the digital domain. Δ-Σ techniques have also been applied to FDC systems [2-4] in different solutions. In [5-7] it is shown that just by oversampling a zero-crossing (ZC) detector with respect to the modulating signal, Δ-Σ equivalent noise-shaping can be achieved. To preserve the increased signal-to-quantization noise-ratio (SQNR) the detector is followed by a Δ-Σ decimator. These systems are referred to as Frequency-ΔΣ-Modulators (FΔΣM's) and provides inherently linear frequency-to-digital conversion.

The basic idea of the FΔΣM is to quantize the angle θ_n by detecting the FM signal zero-crossings positions. This is done by counting the number of ZC's during a fixed time interval $1/f_s$ and reading this number via a register at e ach clock sample (Fig. 1).

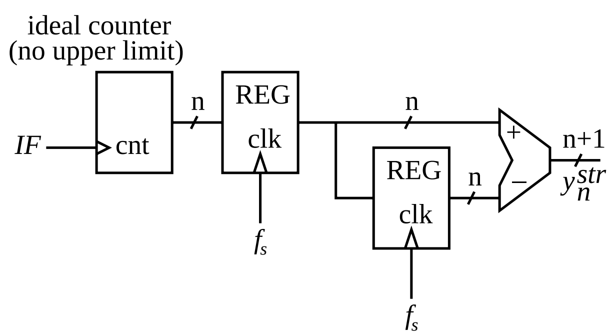

Figure 1: *The basic FDSM sceme.*

By representing the FM angle by the total number of ZC's we introduce an error (e_n) as θ_n now is decribed by $\theta_n = 2\pi(N_n^{ZC} + e_n)$ where N_n^{ZC} is the total number of received ZC's (Fig. 2).

As θ_n is the integral of the modulating signal the quantized phase N_n^{ZC} is digitally differentiated to obtain frequency information (Fig. 1). Due to the differentiation the output signal can be described by $y_n^{str} = \frac{\theta_n}{2\pi} - frac\theta_{n-1}2\pi - (e_n - e_{n-1})$. For f_s much higher than the Nyquist frequency of $m(t)$ (high oversampling) the output can from Eq.XX be approximated by $y_n^{str} = \frac{f_c}{f_s} + \frac{k}{f_s}m(t) - (e_n - e_{n-1})$ where k is the frequency sen sitivity of the frequency modulator. As we see $m(t)$ is just scaled and biased while the quantization error is first-order Δ-Σ noise-shaped.

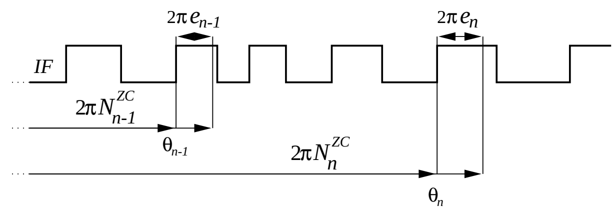

Figure 2: *FM angle θ_n represented by total number of ZC's.*

However, this sceme is based on counting the total number of ZC's which in theory requires a counter with a very high upper limit. A more practical implementation is based on modulo arithmetic [1] where the counter wrap-around error is corrected by the la ck of carry from the corresponding modulo differentiator.

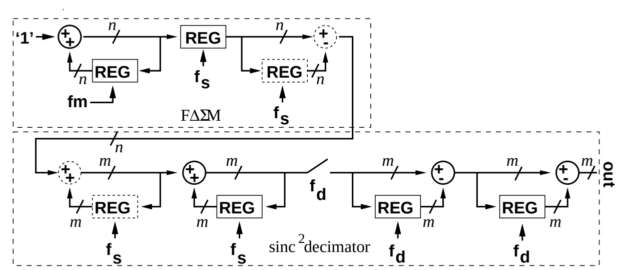

Figure 3: *A modulo-2^n FDSM together with a modulo-2^m decimator..*

In Fig. 3 a modulo-2^n FΔΣM followed by a modulo-2^m sinc^2 decimator [8] is shown. The FΔΣM is an oversampled ZC counting FDC where the phase-detector is modeled as an asynchronous modulo-2^n counter clocked by the rising edge (ZC) of the limited FM signal. The detected quantized phase is then synchronized with the high-speed clock f_s and feed to the modulo-2^n differentiator to obtain frequency information. The output from the FΔΣM is a n-bit Δ-Σ word-stream where each word is the number of positive ZC during the measuring time interval $1/f_s$. If $1/f_s$ is smaller than halve the minimum FM period the

F$\Delta\Sigma$M's output is a Δ-Σ bit-stream.

The triangularly weighted ZC counting technique: For a F$\Delta\Sigma$M the minimum word-length n is a function of the maximum frequency deviation Δf of the FM signal divided by f_s. The minimum word-length m for the following decimator will normally be much larger than for the F$\Delta\Sigma$M. However, by setting $n = m$, the F$\Delta\Sigma$M's differentiator will be the inverse of the following accumulator and the two blocks may be removed (Fig. 4). Since both of these block where clocked by the full clock frequency f_s the total power consumption will be reduced significantly.

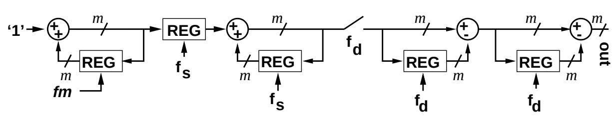

Figure 4: *A triangularly weighted ZC counting FDC (reduced F$\Delta\Sigma$M system).*

The new circuit is a sinc^2 decimator where the first accumulator is clocked by the rising edge of the asynchronous FM signal. The SQNR will be equivalent to the SQNR of the traditional F$\Delta\Sigma$M system which from [6,7] is given by

$$\text{SQNR(dB)} = 20\log\left(\frac{2\Delta f}{f_s}\right) - 20\log\left(\frac{\sqrt{2}\pi}{3}\left(\frac{f_N}{f_s}\right)^{\frac{3}{2}}\right), \quad (1)$$

where f_N is the Nyquist frequency of the modulating signal. The first term is the resolution of an ordinary positive ZC counting FDC and the second term represents the increased resolution resulting from the Δ-Σ noise-shaping.

To understand the operation of the new circuit we may start by comparing it to a traditional ZC counting FDC where the output is the number of positive FM ZC during a low-frequency sampling period $T_d = 1/f_d$. The counting operation is equivalent to dividing T_d into small nonoverlapping sub-intervals of length $T_s = 1/f_s$ and counting the number of positive ZC in each T_s interval, multiply each number by one and add the results together to form the overall sum. The positions of the ZC during T_d are equally weighted as an uniform windowing function have been applied (Fig. 5 top).

The output of the circuit in Fig. 4 can from [8] be expressed as

$$out_n = \sum_{k=1}^{D}\sum_{l=1}^{D} x_{D(n-2)+k+l}, \quad (2)$$

where $x_{D(n-2)+k+l}$ here is the number of positive ZC in sub-interval $D(n-2)+k+l$ and $D = f_s/f_d$ is the decimation ratio. If the sinc^2 decimator is followed by a LP filter f_d will normally be chosen as $4f_N$ [1]. As an example for $D = 4$ one output sample is given by $out_1 = x_{-2} + 2x_{-1} + 3x_0 + 4x_1 + 3x_2 + 2x_3 + x_4$. From this we notice that the new circuit operates by dividing the counting interval $2T_d$ into $2D-1$ sub-intervals, then counts the number of positive ZC in each sub-interval, multiply each number by the corresponding value in a triangularly weighted

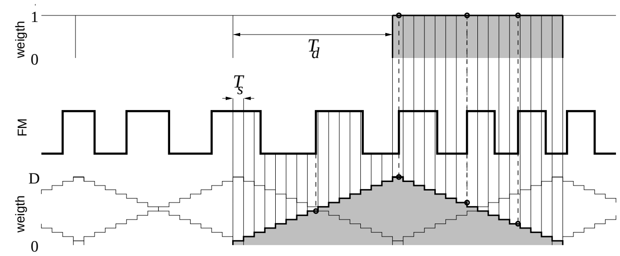

Figure 5: *Uniformly weighted (top) versus triangularly-weighted (bottom) ZC counting.*

window and sums the results providing the overall output (Fig. 2 bottom). In other words, by exchanging the inherently uniform windowing function in the traditional counting FDC by a triangular window, first-order Δ-Σ noise-shaping is achieved. However, by doubling the oversampling ratio or the number of sub-intervals, the SQNR is only increased by $\approx$ 3 dB as the internal signal range in the converter is halved [6,7].

Measured results: A triangularly weighted FDC is intended to be used in a measurement system together a FM output sensor with the following specifications: f_c =610 KHz, Δf = 60KHz and a maximum modulating signal frequency f_m = 500 Hz (f_N = 1 KHz). The required digital resolution is 70dB. A prototype converter have been implemented in TTL running at f_s = 4 MHz (Fig. 6). To avoid glitches, the FM signal was synchronized with f_s prior to first-step accumulation. This is possible since the sampling frequency is much higher than $f_c + \Delta f$. A decimator word-length of 16 bit was found sufficient.

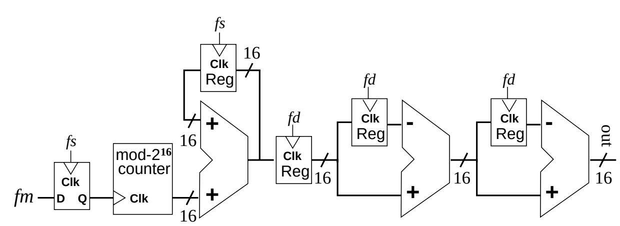

Figure 6: *A triangularly weighted FDC implemented by a sinc^2 decimator.*

A FM signal modulated by a single sinusoidal signal of 271 Hz was provided by a set of HP8116A / HP3245A signal generators. The measured output power spectrum is shown in Fig. 7 for a decimation ratio $D = 16$. From the plot we recognize the shaped quantization error resulting from the Δ-Σ conversion. For frequencies higher than $\approx$10KHz there are some excess noise probably due to the location of the very narrow internal signal range $(f_{carrier} \pm \Delta f)/f_s$ = [0.1375, 0.1675] relative to the equivalent quantization levels 0, 1. For frequencies lower than $\approx$1 KH a noise floor with harmonic distortion corresponding to the spectrum of the signal generator itself appears.

The measured output power spectrum for $D = 1000$ is shown in Fig. 8. In this case the output word rate f_d is 4 KHz. If the converter output is properly LP filtered the SQNR should theoretically from Eq. 1 be 74 dB. However, due to noise assumed to originate from the signal generator itself the measured SNR was found to be 56dB.

(Power compared to full FDSM system)

Conclusion:

Two high speed blocks may be removed since FM is almost bitstream - lowerer power - linear convertion .

We have shown that by introducing a triangular window in the traditional ZC counting FDC, Δ-Σ noise-shaping and decimation results. A simple way to implement the windowing function is by using a double modulo counter or a sinc^2 decimator. By in this way using a Δ-Σ decimator as a ZC counting FDC a higher digital resolution can be achieved than by using a standard count-and-dump FDC as the quantization error is noise-shaped.

Sayfe-Dutta:

$$\widehat{m}_n = \frac{T_{fm}/2}{T_{clk}} = \frac{f_{clk}}{2(f_c + km_n)} \tag{3}$$

$$SR_o = \frac{f_{clk}}{2(f_c - \Delta f)} - \frac{f_{clk}}{2(f_c + \Delta f)} \approx \left(\frac{f_{clk}\Delta f}{f_c^2}\right), \quad \Delta f \ll f_c \tag{4}$$

$$P_{signal} = 20 \log \left(\frac{f_{clk}\Delta f \sqrt{2}}{f_c^2}\right) \tag{5}$$

$$P_{noise} = 20 \log \left(\frac{e_{rms}^{noise}}{\sqrt{\text{OSR}}}\right), \quad e_{rms}^{noise} = \frac{1}{\sqrt{12}} \tag{6}$$

$$\text{SQNR(dB)} \approx 20\text{log} \left(\frac{f_{clk}\Delta f \sqrt{2}}{f_c^2}\right) - 20\text{log} \left(\frac{1}{\sqrt{6}} \left(\frac{f_m^{max}}{f_c}\right)^{1/2}\right) \tag{7}$$

Acknowledgement We would like to thank the Research Council of Norway (NFR) for financially supporting the project.

Mats E. Høvin, Tor S. Lande, Dag T. Wisland *(Department of Informatics, University of Oslo, Blindern, N-0316 Oslo, Norway, matsh@ifi.uio.no)*

Sayfe Kiaei *(Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR 97331, USA, kiaei@ece.orst.edu)*

References

[1] Candy, J.C and Temes, G.C.: *Oversampling delta-sigma data converters*, IEEE Press, New York, 1992.

[2] Riley, T.A.D., Copeland, M.A. and Kwasniewski, T.A.: "Delta-sigma modulation in fractional-*N* frequency synthesis", *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553-559, May 1993.

[3] Beards, R.D. and Copeland, M.A.: "An oversampling delta-sigma frequency discriminator", *IEEE Trans. on Circuits and Systems*-II, vol. 41, no. 1, pp.26-32, Jan. 1994.

[4] Galton, I.:"Analog-input digital phase-locked loops for precise frequency and phase demodulation", *IEEE Trans. on Circuits and Systems*-II, vol. 42, no. 10, pp.26-32, Oct. 1995.

[5] Høvin, M., Olsen, A., Lande, T.S. and Toumazou, C.: "Novel second-order $\Delta - \Sigma$ modulator / frequency-to-digital converter", *IEE Electronics Letters*, vol. 31, no. 2, pp.81-82, 1995.

[6] Høvin, M., Olsen, A., Lande, T.S. and Toumazou, C.: "Delta-sigma converters using frequency modulated intermediate values", *Proc. IEEE ISCAS'95*, pp.175-178.

[7] Høvin, M., Olsen, A., Lande, T.S. and Toumazou, C.: "Delta-sigma modulators using frequency modulated intermediate values", *IEEE J. Solid State Circuits*, vol. 32, no. 1, Jan. 1997. .

[8] Chu, S. and Burrus, C.S.: "Multirate filter designs using comb filters", *IEEE Trans. on Circuits and Systems*, vol. CAS-31, pp. 913-924, Nov. 1984.

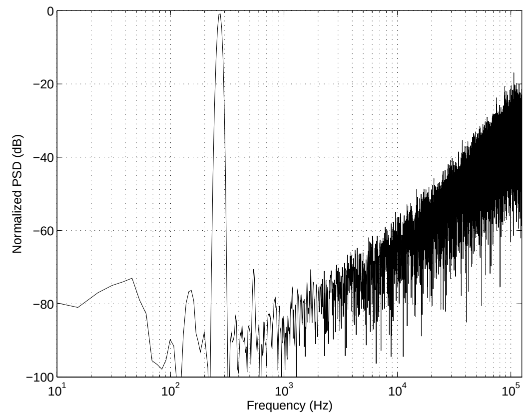

Figure 7: *Measured output spectrum for a 271 Hz sinusoidally modulated FM input signal estimated by* 2^{15}*-point FFT,* $D = 16$. *(Blackman data window)*

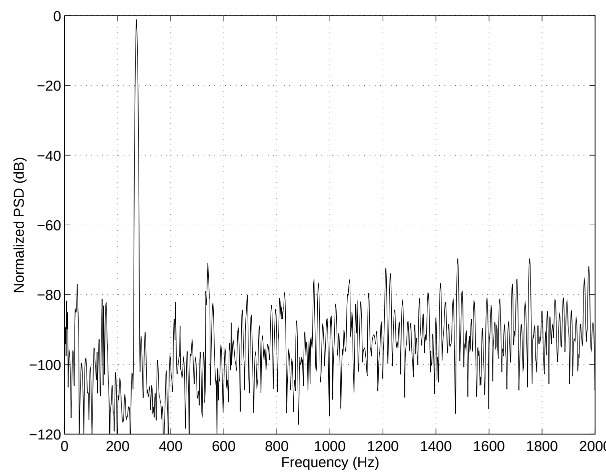

Figure 8: *Measured output spectrum for a 271 Hz sinusoidally modulated FM input signal estimated by* 2^{11}*-point FFT,* $D = 1000$. *(Blackman data window)*