A New Multiport Memory for High Performance Parallel Processor System with Shared Memory

K.Hirano, T.Ono, H.Kurino and M.Koyanagi
Intelligent System Design Lab.
Dept. of Machine Intelligence and Systems Engineering
Graduate School of Engineering, Tohoku University
Aramaki, Aoba-ku, Sendai 980-77 Japan
hirano@sd.mech.tohoku.ac.jp

Abstract— We describe a new multiport memory which is called Shared DRAM(SHDRAM) to solve bus-bottle neck problem in parallel processor system with shared memory. This SHDRAM has four ports. Therefore four processors can be directly connected to this memory without bus-bottle neck. The basic operation of SHDRAM is confirmed by computer simulation and measurement results.

I. Introduction

The parallel processing using multi-processors is very effective to dramatically improve the computational throughput. It is well known that a shared memory is very useful to build the high performance parallel processor system with simple configuration and architecture. However, the bus-bottle neck is a very big problem in the conventional system using a shared memory with common buses. To solve such bus bottle-neck problem, the processors have to be connected directly to the shared memory without using common buses. In such system, each processor can access the shared memory independently of other processors. This paper describes a new multiport memory called Shared DRAM(SHDRAM) which is used as a direct shared memory in high performance parallel processor system.

II. SHDRAM Architecture

A configuration of 2D-SHDRAM with four ports is shown in Fig.1. This memory is basically DRAM with four mats configuration. In 2D-SHDRAM, flip-flop type sense amplifiers of each memory mat are connected by many short buses (broadcast buses) for broadcasting the data. The data transfer speed in these short buses are extremely high because they are internal buses. A processor is connected to each memory mat through sense amplifiers. The data written to the sense amplifiers in some mat by the respective processor are simultaneously transferred (broadcast) to the sense amplifiers in other mats through the broadcast buses. The data transferred to the sense amplifiers are simultaneously written into the DRAM memory cells which belong to the respective memory mats. Therefore, the memory cells with an identical memory address in all memory mats of 2D-SHDRAM have an identical data after the data transfer. These identical data can be read-out simultaneously and independently by four processors. Therefore, this 2D-SHDRAM acts as a direct shared memory without bus-bottle neck. A sense amplifier acts as a cache memory as well as an amplifier to amplify the signal voltage read-out of the DRAM memory cell in 2D-SHDRAM. Therefore, it can be also considered that four cache memories are connected each other by high speed internal buses without a bus bottleneck in 2D-SHDRAM.

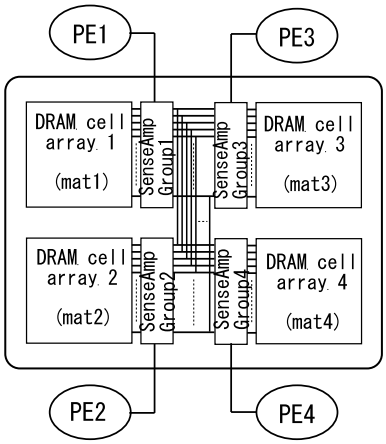

Fig. 1. A configuration of 2D-SHDRAM.

III. Data Sharing Mode of SHDRAM

Several kinds of modes for sharing the data are available in 2D-SHDRAM. Here, we explain an overlaid data mode. In this mode, the shared data are overlaid to four memory mats. Therefore, four memory mats have the identical data. Four groups of sense amplifiers have the identical data as well in this mode. Consequently, the shared data are always consistent among four memory mats and among four groups of sense amplifiers. An example of the operational sequences and simulated waveforms for the overlaid data mode is shown in Fig.2 where a half part of 2D-SHDRAM is illustrated in each step. Each group of sense amplifiers and each memory mat are divided into several blocks as shown in this figure. The step ⓪ in the figure means the initial state. In this ex-

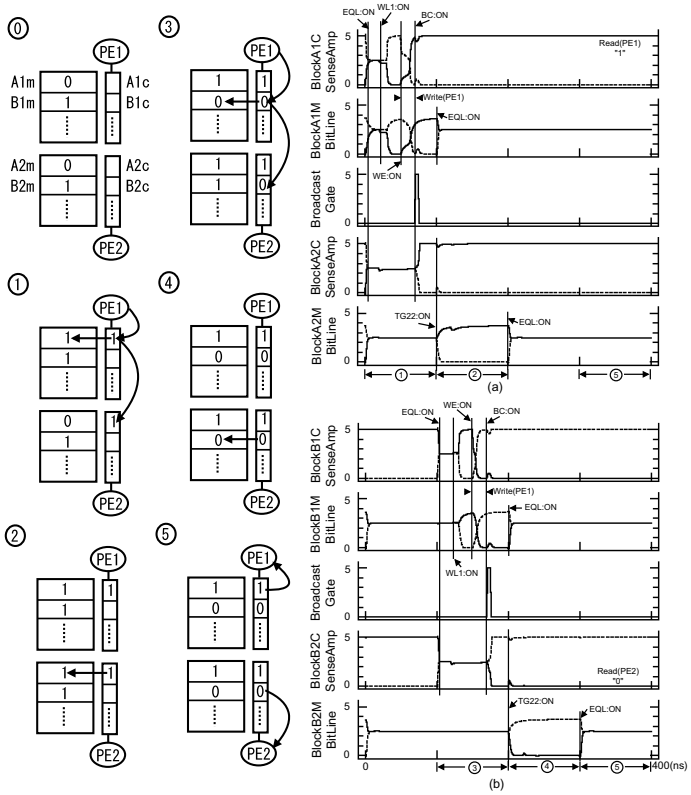

Fig. 2. Simulated waveforms for the overlaid data mode.

ample, the data "0" is stored in A block of memory mat and the data "1" in B block of memory mat. Then, the data "1" are written to A1m block through A1c block by the processor element PE1 in the step ①. Simultaneously, the data "1" written into A1c block is transferred to A2c block through the internal bus. In the step ②, the data in A2c block is written into A2m block. In the step ③ and ④, the data "0" is written by PE1. Thus, two memory mats and two sense amplifier groups become to have the identical data. Therefore, they can act as shared memories. Two processor elements, PE1 and PE2, read the data independently without a conflict in the step ⑤. It is clear from the figure that the overlaid data mode is successfully executed.

IV. Chip Design and Measurement results

We designed a test chip of 2D-SHDRAM with full custom method using 1.5μm 2-level metal CMOS technology. One memory mat consists of 8192 bit DRAM cell array. Each memory mat has own address decoder and I/O circuits. Four mats are integrated into a 4.8×4.8mm chip size. The microphotograph of 2D-SHDRAM is shown in Fig.3. Figure 4 is the measurement waveforms of this test chip. At first, the data "0" is written to A1m block through A1c block. The data is transferred to A2c block and written to A2m block. Next, data "1" is written into A1c block and A2c block by PE1. Then, data "0" in A1m block and A2m block is simultaneously read-out to A1c

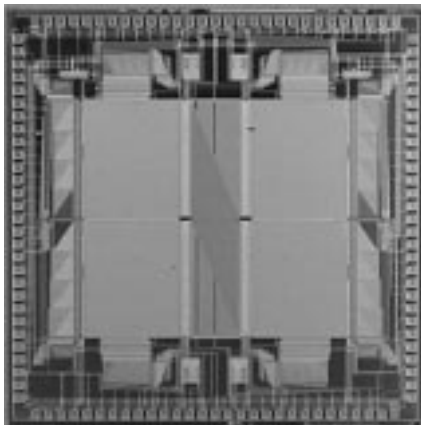

Fig. 3. Microphotograph of 2D-SHDRAM test chip.

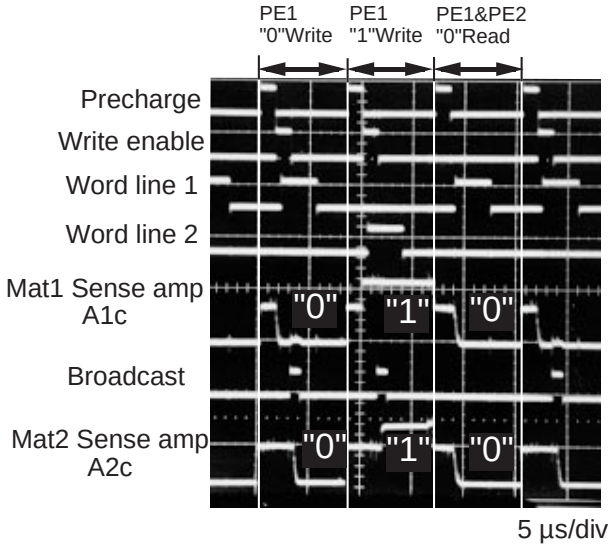

Fig. 4. Measurement waveforms for the overlaid data mode.

block and A2c block. It is clearly seen that overlaid data mode operation are successfully executed in this test chip.

V. Summary and Conclusions

We proposed a new multiport memory, which is called SHDRAM for a high performance parallel processor system with direct shared memory. It was also shown that 4 processors can be directly connected through this SHDRAM. Furthermore, 32768 bit SHDRAM test chip has been fabricated by 1.5μm CMOS technology. The basic operation and the broadcast operation of such SHDRAM were confirmed.

Acknowledgements

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