Design of Digital Neural Cell Scheduler for Intelligent IB-ATM Switch

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Abstract— We present the architecture of the ATM banyan switch composed of pattern process and high-speed digital neural cell scheduler. An input buffer type ATM switch with a window-based contention algorithm is proposed, modeling in VHDL for high-speed cell scheduler of ATM switching. A digital hopfield neural cell scheduler which has the ability of real-time processing is used to solve loss of throughput due to head-of-line(HOL) and internal blocking when FIFO queueing is employed at the Banyan network. In this scheduler, it is found we can minimize the delay for scheduling and select non-blocking cells in maximum leading to high performance. Our proposed ATM switch is modeled in VHDL, synthesized, implemented into a FPGA chip set and fabricated using 0.6§ -CMOS technology.

I. Introduction

The switch system of multistage scheduler from call admission controller system is generally composed of multiplexing, demultiplexing device and controller portion among input[1], output process and switch network where the switch system is classificated by buffering as input buffer, output buffer, shared buffer. The most important factor that decide the ATM switch performance and maximum performance is estimated about input link definitions as transactioned cell number at one cell time slot. Input buffer typed ATM switch need not to raise output process rate under output blocking, and have advantage of salability. Banyan network has the advantage of self-routing. This means that the route through the switch is not determined by a global controller, but rather that each switching element in the network can look at a single bit of the route tag address and decide how it will route the cell. However, the banyan network is blocking, which can occur in two cases, their cells will be routed to the same destination address, their cells will be routed to the same output at the same time. In this paper accept fully the merit of input buffer typed to improve maximum throughput of switch, select windowing method that decrease input buffer size and design hopfield neural network as cell scheduler of complex implementation. So have specific property like simplicity, real time processing. also Token, Circular cell processing is employed at preprocessing that enable bit processing. Cell scheduler is managed easily through optimization rather than other windowing neural cell scheduling algorithm[6][7][8] and can select maximum cells.

II. Proprosed Network and Methodology

Banyan switch is MIN(multiple interconnection network) that enable self-routing at ATM switch[3][4].

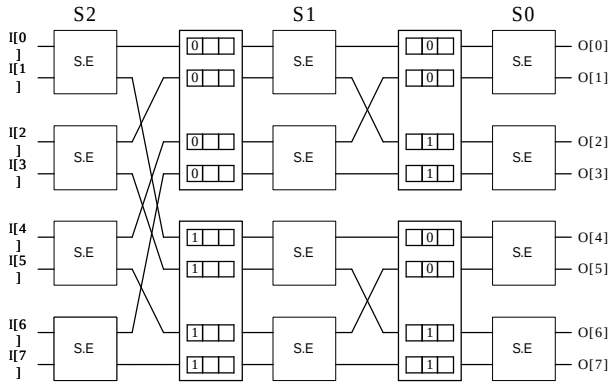

Fig. 1. 8X8 Banyan switch

If the tag bits of two input port at switch element are same mutually by comparison occur blocking, if not same mutually, input cell route upper output port in case of tag bit is 0, route lower output port in case of tag bit is 1. When S.E is connected like Fig. 1, cells find output port of itself without global routing control. Fig.2 is the total block diagram that is proposed in this study. From Fig.2, designed switch have the FIFO.

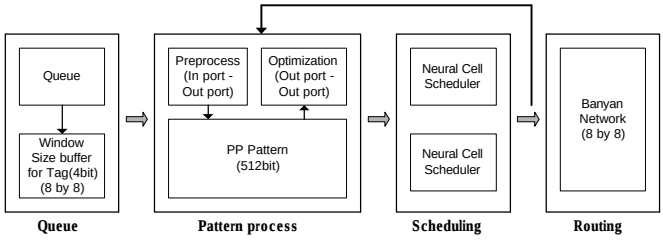

Fig.2.A proposed input-buffer typed ATM switch.

The purpose of optimization is for cells to be transmitted safely to destination address, if cells avoid internal blocking and output blocking at banyan switch when cells come inside

first S.Es queue as input buffer and temporary buffer for storage of cell tag and cell data. Example of operation of preprocess and optimization is given in Fig. 3(a) and Fig. 3(b).

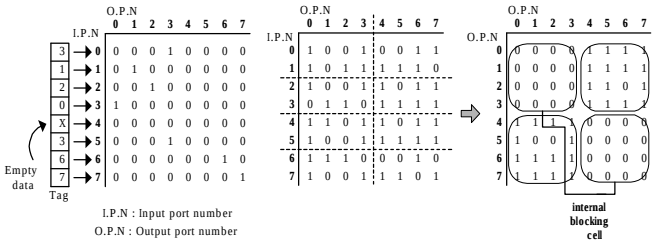

Fig. 3. (a) Preprocessing, (b) Optimization of Input-Output mapping.

However since pattern processing don't include cell position and count, need to store cell position and count value in pattern table as windowing size as when cells pass through preprocessing and optimization. Using the method of recursive neural cell-pattern processing between pattern processing and cell schedulers is algorithmically designed. The cell scheduling is formulated from non-linear optimization problem and is operated by the means of the same principles what solving TSP(Traveling salesman problem). But difference is not to search for minimum distance using distance value but maximum cell number that avoid output-blocking using binary pattern of optimization without internal-blocking. In this paper, neural network is Hopfield network that is composed of 16 neuron.

III. Results and Discussions

The ATM switch is modeled in VHDL, synthesized, and implemented into a FPGA chip set[5]. Synthesis of the neural cell scheduler circuit as shown in Fig. 4. The function blocks are modeled in VHDL and verified by simulation and synthesis. Gate counts for the finalized scheduler module are about 6000 and layout with 0.6§ -TLM(Triple Layer Metal) CMOS technology using Mentor CAD tool has 80 pins including grounds and suppliers. The schematic of recursive neural pattern processing from synthesized and implemented results as shown in Fig. 5 shows the simulation of recursive neural pattern processing as expected. The final layout of the chip using back-end CAD tool, Mentor, indicated error-free checking as shown in Fig. 6, which is under fabrication process at LG fab-site.

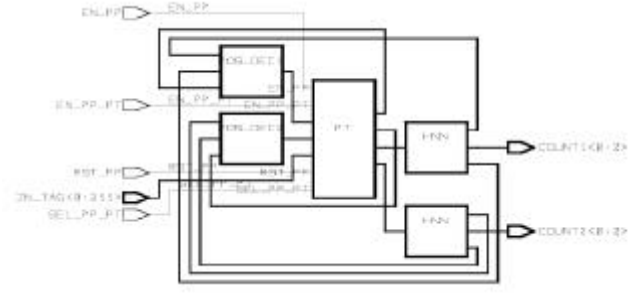

Fig. 4. Synthesized result for IB-ATM switch.

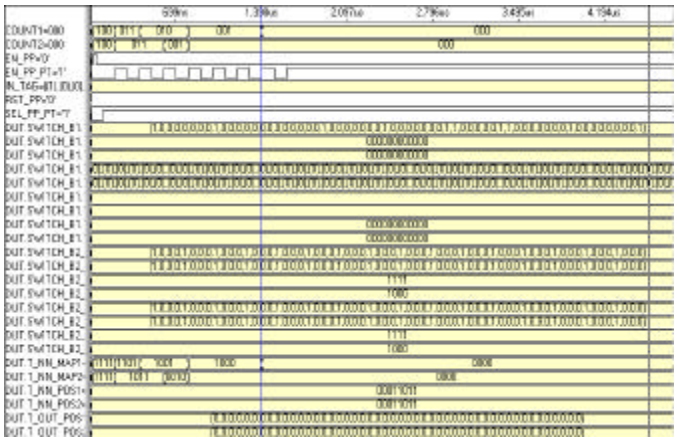

Fig. 5. Simulation results of a neural cell scheduler using Verilog-XL.

IV. Conclusion

This paper is to improve throughput through pattern process and high-speed cell scheduler. is proposed. Especially in case of pattern process, preprocess and optimization is decrease load of neural cell scheduler. High speed is expected when this architecture is connected by parallel in queue. In the proposed scheduler, we minimized the delay for scheduling and select non-blocking cells in maximum leading to high performance.

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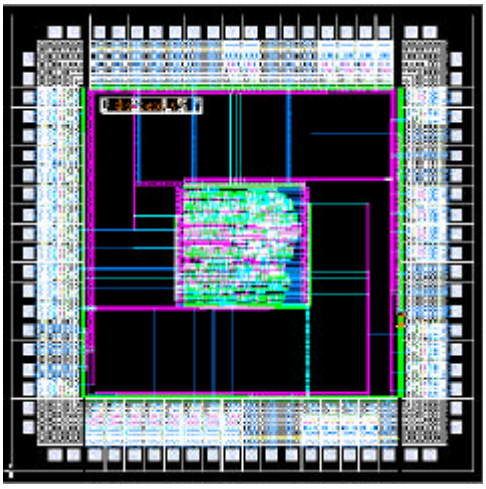

Fig. 6. The layout with 80-pin of the chip.