A High-Speed PLA using Array Logic Circuits with Latch Sense Amplifiers and a Charge Sharing Scheme

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Abstract— In this paper, a high-speed PLA based on latch sense amplifiers and a charge sharing scheme is presented. The circuit consists of logic cell arrays, dual-rail bit-lines, latch sense amplifiers, and control blocks. By latch sense amplifiers, a read-out scheme sensing the differential voltage of dual-rail bit-lines caused by charge sharing is used for high-speed operation. As an application of the proposed PLA, a 32-bit binary comparator is designed and implemented in a 0.6-μm double-poly, triple-metal CMOS process. Results of HSPICE simulation are 2.9 times faster than the conventional CMOS circuit. The measured results show a good agreement with the simulation.

I. Introduction

Programmable logic arrays (PLAs) are widely used for combinational and sequential logic circuits in VLSI systems because of its simplicity, regularity, and flexibility. Often, microprocessors use PLAs to implement such functions as instruction decoding. The regularity in the physical structure well suits the VLSI design.

This paper proposes a high-speed PLA using array logic circuits with latch sense amplifiers and a charge sharing scheme. Latch sense amplifiers, which are commonly used in memory-type circuits, amplify small voltage differences between bit-lines to a rail-to-rail signal. Meanwhile, some logic circuits take advantage of the high-speed read-out capabilities of sense amplifiers [1], [2]. The dynamic array logic circuits in [2] can achieve a high-speed circuit operation using sense amplifiers. However, logic functions that can be realized are limited to only AND functions. Besides, discharging speed of the bit-lines depends on the number of activated word-lines, so that it takes a long cycle time due to precharge.

The present circuit can realize any logic function using PLA structure and control blocks. Moreover, by using a charge sharing scheme, the voltage swing of the bit-lines is reduced for high-speed and low-power operation.

II. PLA Configuration

Fig. 1(a) shows a basic cell of the proposed PLA. This circuit is an OR-NOR logic configuration based on a dual-rail bit-line and a latch sense amplifier. The output signals, OR and NOR, are obtained by sensing the differential voltage of the dual-rail bit-line. The X_1 to X_n signals, which are called word-lines, are primary inputs or their negates. The REF signal is the reference word-line. The DC signal discharges the virtual ground VG. The PC signal precharges and equalizes the bit-lines, BL and $\overline{\text{BL}}$, to V_{dd}. The ISO signal isolates the sense amplifier from the bit-lines. The SAE signal activates the sense amplifier. When a word-line is activated, the real transistor (Q_{real}) pulls BL down. Otherwise BL stays high. By the reference transistor (Q_{ref}), $\overline{\text{BL}}$ is pulled down slowly in comparison with BL every read-out cycle. The purpose of the dummy transistor (Q_{dum}) is to load-balance BL

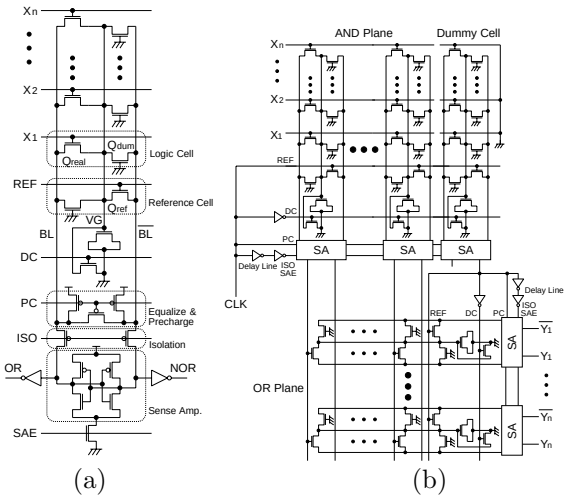

Fig. 1. (a)Basic cell of PLA and (b)schematic of the proposed PLA.

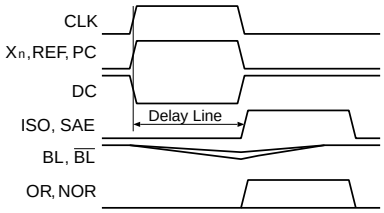

Fig. 2. Timing diagram of control signals.

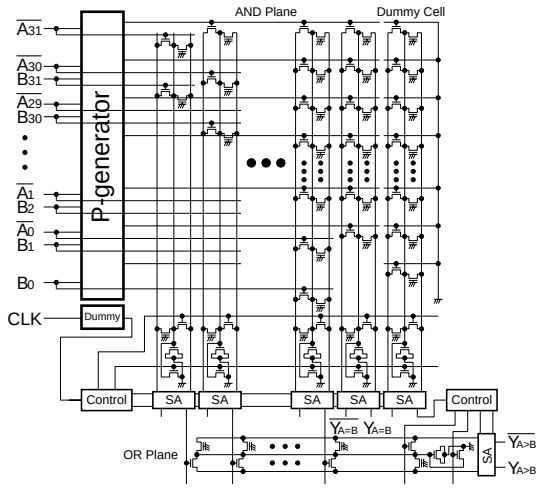

Fig. 3. Schematic of the proposed 32-bit binary comparator.

and $\overline{\mathrm{BL}}$. The VG is the virtual ground using a MOS capacitor. The charge of the bit-lines is shared with VG. As a result, BL and $\overline{\mathrm{BL}}$ are not completely discharged. Thus, this enables BL and $\overline{\mathrm{BL}}$ to be precharged faster.

Fig. 1(b) and Fig. 2 show the schematic of the proposed PLA and a timing diagram of control signals, respectively. An array of the basic cells is used as an AND plane or an OR plane. Control signals of the AND plane (i.e., PC, SAE, and so forth) are generated from the CLK signal using a delay line of a chain of inverters. On the other hand, control signals of the OR plane are generated from the output signal of the dummy cell and a delay line of a chain of inverters. The sizes of these inverters of delay lines should be designed depending on the number of inputs (e.g., 64-bit, 32-bit, or 16-bit). The output signal of the dummy cell is activated every read-out cycle and tracks the output signals of the AND plane across operating conditions and process variations.

III. Design of 32-bit Binary Comparator

As an application of the proposed PLA, a 32-bit binary comparator is designed and implemented in a 0.6-μm double-poly, triple-metal CMOS process with a supply voltage of 5V. Logic functions of an equality and magnitude comparator of two 32-bit binary numbers, A and B, are expressed as

$$P_n = A_n \cdot B_n + \overline{A_n} \cdot \overline{B_n} = \overline{A_n \oplus B_n} \quad (1)$$

$$Y_{A=B} = P_{31} \cdot P_{30} \cdot \cdots \cdot P_2 \cdot P_1 \cdot P_0 \quad (2)$$

$$\begin{aligned} Y_{A>B} = {} & A_{31} \cdot \overline{B_{31}} \\ & + P_{31} \cdot A_{30} \cdot \overline{B_{30}} \\ & + P_{31} \cdot P_{30} \cdot A_{29} \cdot \overline{B_{29}} \\ & + \cdots \\ & + P_{31} \cdot P_{30} \cdot \cdots \cdot P_3 \cdot P_2 \cdot A_1 \cdot \overline{B_1} \\ & + P_{31} \cdot P_{30} \cdot \cdots \cdot P_2 \cdot P_1 \cdot A_0 \cdot \overline{B_0} \end{aligned} \quad (3)$$

where $Y_{A=B}$ is high when $A = B$, while $Y_{A>B}$ is high when $A > B$. The schematic for this implementation is shown in Fig. 3. The propagation signals P_n are generated by XOR gates located in the P-generator.

Results of HSPICE simulation are shown in Table I. The output signals, $Y_{A=B}$ and $Y_{A>B}$, are respectively 2.93 and 1.56 times faster than those of the conventional CMOS random logic circuits using carry look-ahead gates. A comparison of area and a designed chip microphotograph are shown in Table II and Fig. 4, respectively. Fig. 5 shows the measured waveforms along the critical path using electron beam probing. The measured results show a good agreement with the simulation.

TABLE I
Simulated Comparison of Delay Time

Function	This Work	CMOS	Speed Improvement
$Y_{A=B}$	0.45 ns	1.32 ns	2.93 times
$Y_{A>B}$	0.90 ns	1.40 ns	1.56 times

TABLE II
Comparison of Area

This Work	CMOS
550μm x 1050μm	905μm x 182μm

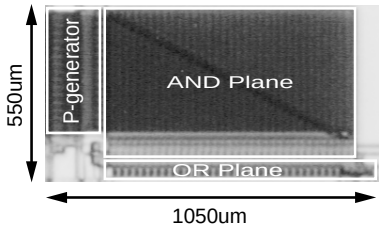

Fig. 4. Chip microphotograph.

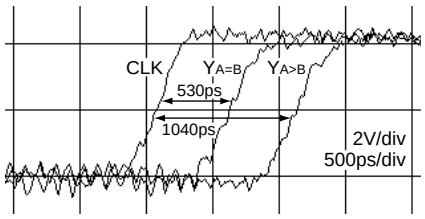

Fig. 5. Measured waveforms.

IV. Conclusion

We have proposed a high-speed PLA using array logic circuits with latch sense amplifiers and a charge sharing scheme. As an application of the proposed PLA, a 32-bit binary comparator is designed and implemented. By taking advantage of the fast read-out capabilities of the present scheme, a high-speed circuit operation has been achieved.

Acknowledgment

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References

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[2] O. Takahashi, N. Aoki, J. Silberman, and S. Dhong, "1GHz Logic Circuits with Sense Amplifiers," in *Symp. VLSI Circuits Dig. Tech. Papers*, 1998, pp. 110-111.