SHORT CIRCUIT POWER ESTIMATION OF STATIC CMOS CIRCUITS

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Abstract - This paper presents a simple method to estimate short-circuit power dissipation for static CMOS logic circuits. Short-circuit current expression is derived by accurately interpolating peak points of actual current curves which is influenced by the gate-to-drain coupling capacitance. It is shown through simulations that the proposed technique yields better accuracy than previous methods when signal transition time and/or load capacitance decreases, which is a characteristic of the present technological evolution.

I. INTRODUCTION

As clock speed increases and function block sizes scale down in today's technology trend, the estimation for power and gate delay need to be fine-tuned. In circuit design flows, the accurate estimation of the power dissipation and gate delay of CMOS gates has become an essential factor for reliability and performance of the chips.

In general, power dissipation in static CMOS circuits is composed of dynamic power dissipation, static power dissipation and short-circuit power dissipation. During the output transition in a static CMOS structure, a direct path from power supply to ground is created, resulting in a short circuit power dissipation that can be more than 20 percent of the total power dissipation since the number of transitions increases due to clock speed-up. Also, the short-circuit current has an effect on the evaluation of propagation delay of CMOS gates. Therefore, estimating the short-circuit current is important to design high-speed VLSI's.

Much effort has been devoted for the extraction of accurate, analytical expressions for timing models of basic circuits. However, previous works in the short-circuit power estimation area have not entirely or exactly reflected gate-to-drain coupling capacitance and the short channel effect [2][3][4][5]. For example, a recent work [6] overlooked the gate-to-drain capacitance effect and required a lot of computational iteration due to the introduction of power series. Hence, we present a macromodel for the estimation of short-circuit power, which enables detailed analysis of the transient behavior of CMOS inverters. We model the short-circuit current by an appropriate linear or nonlinear function, in order to achieve better accuracy and to avoid an overestimation of short-circuit power dissipation, with taking the influence of the gate-to-drain coupling capacitance into account.

II. ANALYSIS OF SHORT CIRCUIT CURRENT IN CMOS INVERTER

Figure 1 illustrates a rising ramp input (eq.(1)) and CMOS inverter model:

$$V_{in} = \frac{V_{DD}}{t_T} t, \qquad 0 \le t \le t_T. \tag{1}$$

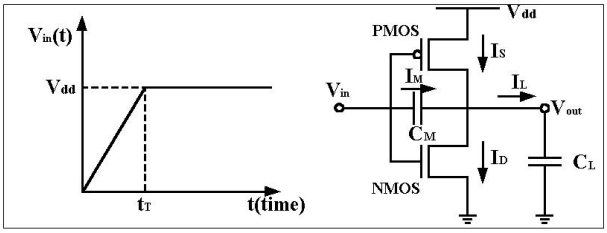


Fig. 1. The ramp input and the CMOS inverter

In Fig. 1, the output load consists of the inverter drain junction capacitance, the gate capacitance of fan-out gates and the interconnect capacitance. The gate-to-drain coupling capacitance C_M is

$$C_M = C_{gdo} + C_g \tag{2}$$

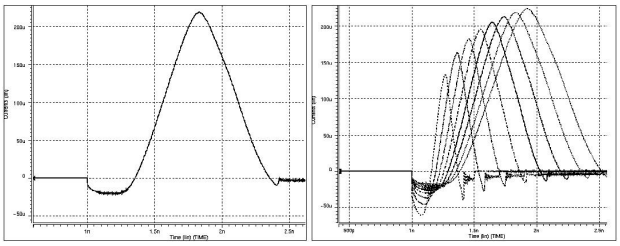
and

$$C_g = C_{gs} + C_{gd} \tag{3}$$

where C_{gdo} is gate-to-drain overlap capacitance, C_g is gate-to-channel capacitance, C_{gs} is gate-to-source channel capacitance, C_{gd} is gate-to-drain channel capacitance and C_{ox} is gate-to-oxide capacitance except overlap.

$$C_{gd} = \frac{1}{2} C_{ox} WL . \quad (4)$$

Figure 2 shows the influence of gate-drain coupling capacitance in short-circuit current waveforms. Note that as transition time decreases the negative portion in Fig. 2 is increasing compared to the positive portion. We model the short-circuit current based on Fig. 2 in the following section.

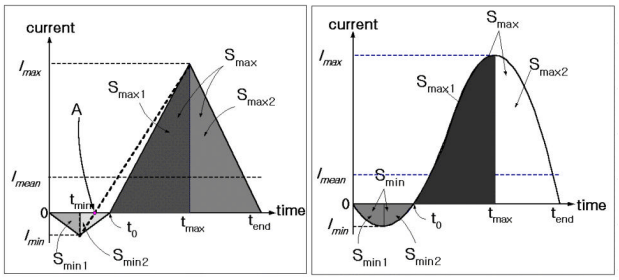


(a) (b)

Fig. 2. HSPICE simulation results of short-circuit currents.
(a) t_T=1.7ns, C_L=30fF
(b) t_T=0.5ns~1.9ns, C_L=30fF (varying input transition time)

III. MODELING THE SHORT CIRCUIT CURRENT

As shown in Fig. 3, we model the short-circuit current waveform from two choices: the piecewise nonlinear modeling and the piecewise linear modeling.



(a) (b)

Fig. 3. Current Modeling Choices
(a) Piecewise linear (b) Piecewise nonlinear

The short-circuit power dissipation caused by a short circuit current I_S during the rising transition of input signal can be estimated as :

$$P_{sc} = I_{mean} \cdot V_{DD} . \quad (5)$$

I_{mean} is the average current and is given by

$$I_{mean} = \frac{(S_{min} + S_{max})}{t_r} = \frac{S_{total}}{t_r} \quad (6)$$

where S_{max} and S_{min} are marked in Fig. 3.

In order to obtain S_{min} and S_{max} values, we model short-circuit current, I_S , according to three methods as follows :

• Method A : Current waveform I_S is modeled by

$$I_s(t) = a_1 t \cdot b_1^{-g_1 t} \quad (7)$$

where a_1, b_1 and g_1 can be obtained by using the peak points and are given by

$$a_1 = \frac{I_{min} b_1^{\frac{1}{\log b_1}}}{t_{min}}, \quad b_1 > 0 \ (b_1 \neq 1), \quad g_1 = \frac{1}{t_{min} \log b_1} .$$

Then, S_{total} is

$$S_{total} = (e\text{-}2)\{t_0 I_{min} + (t_{end} - t_0) I_{max}\} . \quad (8)$$

• Method B : I_S is modeled by

$$I_s(t) = a_2 t \cdot b_2^{-\frac{t^2}{r_2}} \quad (9)$$

where a_2, b_2 and g_2 can be obtained using the similar way in Method A and are given by

$$a_2 = \frac{I_{min} b_2^{\frac{1}{2\log b_2}}}{t_{min}}, \quad b_2 > 0 \ (b_2 \neq 1), \quad g_2 = \frac{1}{t_{min} \log b_2} .$$

Then S_{total} is

$$S_{total} = (\sqrt{e}\text{-}1)\{t_0 I_{min} + (t_{end} - t_0) I_{max}\} . \quad (10)$$

• Method C : I_S is modeled by

$$I_s(t) = a_3 t \quad (11)$$

where a_3 is

$$a_3 = \frac{I_{min}}{t_{min}} .$$

Then, S_{total} is given by using the triangle area formula :

$$S_{total} = 0.5 \ \{t_0 I_{min} + (t_{end} - t_0) I_{max}\} . \quad (12)$$

Since we use four linear equations, Method C is more accurate than the method presented in [2].

Consequently, for the accurate estimation of short-circuit power, unknown values t_{min}, I_{min}, t_{max} and I_{max} have to be calculated as exactly as possible. In this derivation process, we use the simplified bulk-charge MOS model[8] for the operational region of MOS devices.

A. Derivation of I_{min}

To obtain I_{min}, we have to investigate the behavior of MOS transistors. At this time point, the NMOS transistor is off, and the PMOS transistor is in the linear region. Therefore, t_{min} is equal to t_{thn} and I_{min} is

$$I_{min} = b_p\left[\left(V_{DD} - \frac{V_{DD}}{t_T}t_{thn} - |V_{thp}|\right)\left(V_{DD} - V_{out}(t_{thn})\right) - \frac{1+d_p}{2}\left(V_{DD} - V_{out}(t_{thn})\right)^2\right]. \quad (13)$$

Also, eq. (14) is derived by applying the Kirchoff's current law at the output node

$$I_s = \frac{dV_{out}}{dt}(C_L + C_M) - \frac{V_{DD}}{t_T}C_M. \quad (14)$$

Substituting equations (7), (9) and (11) for eq. (14), $V_{out}(t_{thn})$ is expressed as linear function of I_{min}:

$$V_{out}(t_{min}) = V_{DD} + \frac{C_M V_{DD}\, t_{thn}}{(C_L + C_M)\, t_T} + \frac{S_{min1}}{(C_L + C_M)} \quad (15)$$

where $V_{out}(t_{thn})$ is the output voltage when the input voltage reaches V_{thn}. Solving eq.(13) and eq.(15), we can obtain I_{min} as follows:

$$I_{min} = \frac{-a_2 - \sqrt{a_2^{\,2} - 4a_1a_3}}{2a_1}. \quad (16)$$

Each parameter in methods A to C is specified in Appendix A and we assume that the value of inner root is always positive.

B. Derivation of I_{max}

To calculate I_{max}, we consider two cases as follows (Case A and Case B). We categorize two cases using the criteria defined in [6].

• Case A : In this case, PMOS transistor is in linear region at t_{max} and NMOS transistor is in saturation region. Thus, I_{max} is given by

$$I_{\max} = b_p\left[\left(V_{DD} - \frac{V_{DD}}{t_T}t_{thn} - |V_{thp}|\right)\left(V_{DD} - V_{out}(t_{\max})\right) - \frac{1+d_p}{2}\left(V_{DD} - V_{out}(t_{\max})\right)^2\right]. \quad (17)$$

To calculate t_0 and t_{max} in eq. (17), we have used the fact that short circuit current is almost symmetric in this case. By applying KCL at ouput node, $V_{out}(t_{thn})$ is derived by a linear equation as follows.

$$V_{out}(t_{max}) = V_{DD} - \frac{b_n t_T (V_{DD}t_{max} - V_{thn})^3}{6V_{DD}(C_M + C_L)(1+d_n)}\left(\frac{V_{DD}t_{max}}{t_T}\right)^3 + \frac{C_M V_{DD}t_{max}}{(C_L + C_M)t_T} + \frac{S_{min} + S_{max1}}{(C_L + C_M)}. \quad (18)$$

Substituting eq. (18) for eq. (17), I_{max} is obtained as solutions of 2nd-order polynomial as follows:

$$I_{max} = \frac{-b_1 - \sqrt{b_2^{\,2} - 4b_1b_3}}{2b_1}, \quad b_2^{\,2} - 4b_1b_3 > 0 \quad (19)$$

and parameters in eq. (19) are specified in Appendix B.

• Case B : In this case, both PMOS and NMOS transistors are in saturation region at t_{max}. By solving the differential equation obtained at output node, $V_{out}(t)$ and I_{max} are expressed by

$$V_{out}(t) = V_{DD} - \frac{b_n t_T (V_{in}(t) - V_{thn})^3}{6V_{DD}(C_M + C_L)(1+d_n)} + \frac{(I_{max} - I_{min})(t - t_{thn})^2}{2(t_{max} - t_{min})(C_M + C_L)} + \frac{I_{min}(t - t_{min})}{C_M + C_L} + \frac{C_M V_{in}(t)}{C_M + C_L} + \frac{S_{min1}}{C_M + C_L}, \quad (20)$$

$$I_{max} = \frac{b_p}{2(1+d_p)}(V_{DD} - V_{in}(t_{max}) - |V_{thp}|)^2. \quad (21)$$

Since t_{max} is the time at logic threshold voltage [14], we can get the following equation.

$$V_{out}(t_{max}) = V_{in}(t_{max}) = V_{INV}. \quad (22)$$

Solving eqs. (20), (21) and (22) together, we get eq. (23) :

$$c_1V_{INV}^3 + c_2V_{INV}^2 + c_3V_{INV} + c_4 = 0 \quad (23)$$

and coefficients are specified in Appendix C. Thus, solving 3rd-order polynomial, eq. (23), I_{max} can be easily derived.

IV. EXPERIMENTAL RESULTS

We examine the accuracy of the short-circuit power estimated using the proposed expression. Figure 5 shows the short-circuit power values estimated by method C, those calculated by the formulas proposed by Vemuru [2] and Veendrick [11], and those simulated by HSPICE. We compare the estimation results of the short circuit power dissipated per one clock cycle as a function of output load capacitance under various input transition times.

It is shown that the error in the results obtained by the proposed method is smaller than that of other works. Note that error ratio is increasing as output load capacitance scales down. Average relative error ratio is 6.5% in the results estimated by the proposed method.

Simulation environment (process technology) is L=0.5μm, W=3.5μm, $|V_{thp}|$=826.92mV, β_p=2.0mA/V^2, δ_p=0.24 in PMOS transistor and L=0.5μm, W=2 μm, V_{thn} =697.82mV, β_n=2.0mA/V^2, δ_n=0.326 in NMOS transistors.

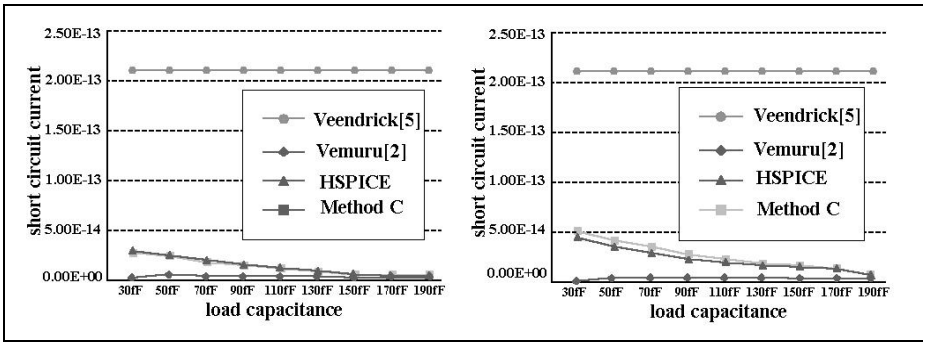


Figure.5. Comparison of various short -circuit power estimation methods and simulation results
(a) transition time = 0.9ns (b) transition time = 1.1ns

V. CONCLUSIONS

In this paper, we have proposed an analytical expression to estimate short circuit power dissipation in CMOS inverters. In this method, we have accurately taken into account the influence of the short-circuit current and the gate-to-drain coupling capacitance. Our method yields better estimation accuracy and computational efficiency than previous works. Specially, when input signal transition time and load capacitance of CMOS gates decrease, it is shown that the results of the proposed method are in good agreement with HSPICE simulation.

VI. APPENDIX

Appendix A

Parameters in Method A are:

$$a_1 = \frac{(1+d_p)(e-2)^2 t_{thn}^{\ 2}}{2(C_L+C_M)},$$

$$a_2 = \frac{1}{b_p} + \frac{t_{thn}(e\text{-}2)}{(C_L+C_M)}\left\{V_{DD} - V_{thn} - |V_{thp}| + \frac{C_M V_{thn}(1+d_p)}{C_L+C_M}\right\},$$

$$a_3 = \frac{C_M V_{thn}}{C_L+C_M}\left\{V_{DD} - V_{thn} - |V_{thp}| + \frac{C_M V_{thn}(1+d)}{2(C_L+C_M)}\right\}. \quad \text{(A -1)}$$

Parameters in Method B are:

$$a_1 = \frac{(1+d_p)(\sqrt{e}-2)^2 t_{thn}^{\ 2}}{2(C_L+C_M)},$$

$$a_2 = \frac{1}{b_p} + \frac{t_{thn}(\sqrt{e}\text{-}2)}{(C_L+C_M)}\left\{V_{DD} - V_{thn} - |V_{thp}| + \frac{C_M V_{thn}(1+d_p)}{C_L+C_M}\right\},$$

$a_3 =$ same as a_3 in Method A. (A - 2)

Parameters in Method C are:

$$a_1 = \frac{(1+d_p)t_{thn}^{\ 2}}{8(C_L+C_M)},$$

$$a_2 = \frac{1}{b_p} + \frac{t_{thn}}{2(C_L+C_M)}\left\{V_{DD} - V_{thn} - |V_{thp}| + \frac{C_M V_{thn}(1+d_p)}{C_L+C_M}\right\},$$

$a_3 =$ same as a_3 in Method A. (A - 3)

Appendix B

Parameters in Method C are:

$$b_1 = \frac{t_1(1+d_p)^2}{4}, \quad \text{(B -1)}$$

$$b_2 = t_1 t_2(1+d_p) + \frac{1}{b_p} + t_1\left(V_{DD} - \frac{V_{DD}t_{max}}{t_T} - |V_{thp}|\right), \quad \text{(B - 2)}$$

$$b_3 = t_2\left\{\frac{(1+d_p)^2}{4} + V_{DD} - \frac{V_{DD}t_{max}}{t_T} - |V_{thp}|\right\} \quad \text{(B - 3)}$$

where

$$t_1 = \frac{S_{max1}}{(C_L+C_M)I_{max}}, \quad \text{(B - 4)}$$

$$t_2 = t_3\left(\frac{V_{DD}t_{max}}{t_T} - V_{thn}\right)^3 + \frac{S_{min}}{C_M+C_L} + \frac{C_M V_{DD} t_{max}}{(C_M+C_L)t_T}, \quad \text{(B - 5)}$$

$$t_3 = -\frac{b_n t_T}{6V_{DD}(1+d_n)(C_L+C_M)}. \quad \text{(B - 6)}$$

Appendix C

Coefficients of eq. (23) are:

$$c_1 = \frac{t_T}{2V_{DD}}\left\{\frac{b_n}{3(1+d_n)} - \frac{b_p}{2(1+d_p)}\right\}, \quad \text{(C-1)}$$

$$c_2 = -\frac{b_n t_{thn}}{2(1+d_n)} + \frac{b_p}{2(1+d_p)}\left\{\frac{t_T(V_{DD}-|V_{thp}|)}{V_{DD}} + \frac{t_{thn}}{2}\right\}, \quad \text{(C-2)}$$

$$c_3 = \frac{b_n t_T V_{thn}^2}{2V_{DD}(1+d_n)} - \frac{I_{min} t_T}{2V_{DD}} + C_L - \frac{b_p(V_{DD}-|V_{thp}|)}{4(1+d_p)}\left\{\frac{t_T(V_{DD}-|V_{thp}|)}{V_{DD}} + 2t_{thn}\right\}. \quad \text{(C-3)}$$

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