Layout Design Methodologies for Sub-Wavelength Manufacturing

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Abstract

In this paper, we describe new types of layout design constraints needed to effectively leverage advanced optical wafer lithography techniques. Most of these constraints are dictated by the physics of advanced lithography processes, while other constraints are imposed by new photomask techniques. Among the methods discussed are 1) phase shift mask (PSM) lithography in which phase information is placed on the photomask in combination with conventional clear and dark information; 2) optical proximity correction (OPC) where predictable distortions in feature geometry are corrected by putting an inverse distortion on the mask; 3) off-axis illumination optics that improve resolution of some configurations at the expense of others; and 4) use of non-resolving assist features that improve neighboring structures.

Keywords

optical proximity correction, OPC, phase shift mask, PSM, lithography.

1. Introduction

In the mid 1990s, as the minimum dimension of chip features approached the wavelengths of the light used to print them, shape distortions from previously ignored proximity effects caused dimensional variations beyond the typical ±10% tolerance limit. One component of the proximity effect is optical interaction among neighboring feature images; other components arise from similar mechanisms in the resist and etch processes. To maintain control of feature dimensions OPC emerged as a necessary component of the lithography process [1] [2]. OPC captures the repeatable variations observed in a lithography process and modifies the mask layout design to counteract predicted distortions (see Figure 1).

Following Moore's Law, chip feature sizes are shrinking at a faster clip than projected wavelength reductions for lithography equipment [3]. Nonetheless, it is commonly accepted that optical lithography will be viable through the 70nm process node. In addition to the many enhancements in equipment, materials, and processes needed to achieve this degree of performance [4], resolution enhancement techniques (RETs), new photomask technologies and mask layout design methods will be required to resolve dimensions far below the illuminating wavelength. Most of these techniques are variations on the alternating phase shift mask, invented in 1982 [5]. The basic principle of phase masks is illustrated in Figure 2.

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Figure 1: OPC counteracts lithography distortions

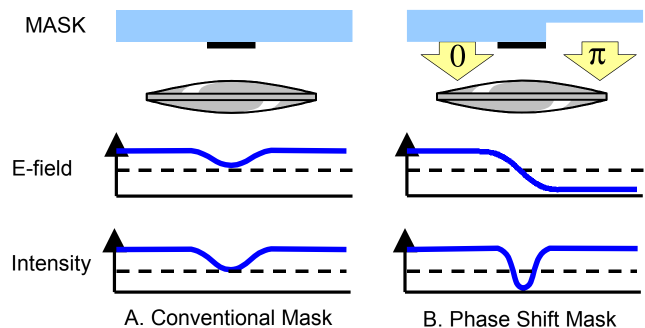

Figure 2: Phase masks resolve smaller lines than conventional masks.

With conventional mask lithography (Figure 2A) lines below a certain size, depending on wavelength and other optical parameters, cannot be resolved. With modulated thickness of transmitting (clear) regions, a phase mask (Figure 2B) shifts the phase of transmitted light 180 degrees relative to light in adjacent regions. Interference between the phased regions projected on the wafer creates a notch in the imaged intensity sufficient to resolve a fine line. Furthermore, the imaged dimension of a PSM line is relatively immune to small variations in focus height.

Many RETs require new geometric constraints not currently enforced in layout designs. The implication for IC layout designers and EDA software suppliers is that new designs must be laid out to comply with RET requirements. In the following, several RET technologies are explained and corresponding layout constraints are outlined. These constraints will be embodied in automated

syntheses, such as cell compactors and compilers, placers and routers, as well as in layout verification tools.

2. Layout compliance for phase shift masks

Layout design requirements for PSM are illustrated in Figure 4. PSM *mapping* is a synthesis operation that derives the shapes and locations of phase mask figures from the layout. Alternating PSM requires that opposing phase regions be placed on opposite sides of every critical line. Furthermore, every phase region must be no smaller than a specified minimum size for it to work. Some configurations, such as the ring of critical features shown in Figure 4, do not allow alternating mapping of phases across every feature while providing phase areas meeting the required minimum size. To use PSM such *cyclic conflicts* must not be present in the design layout. Graph techniques may be used to optimally remove cyclic conflicts from layout designs [6]. The most likely modification is to increase the spacing between any one of the pairs of lines so that two properly sized phase regions can be placed between them. An alternative, if possible, is making one of the lines non-critical, hence larger, so that it will safely image without the phase shift effect.

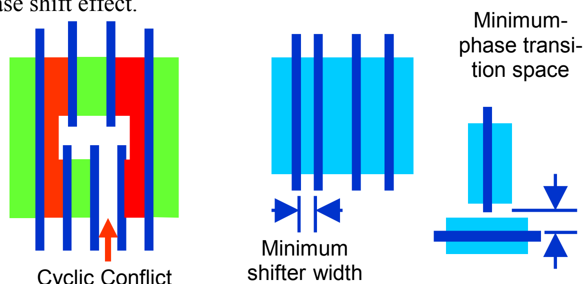

Figure 4: Design layout constraints for Alternating PSM

A dark line will always be imaged by a PSM wherever phase regions meet. In general, a PSM layout will have places where a change in phase, a *phase transition*, is needed, but where no line is wanted. Unwanted dark lines and regions can be removed by a second exposure with a conventional, *trim* mask. The design layout must anticipate where phase transitions can occur and provide sufficient spacing in these locations to allow trim features to resolve and align properly.

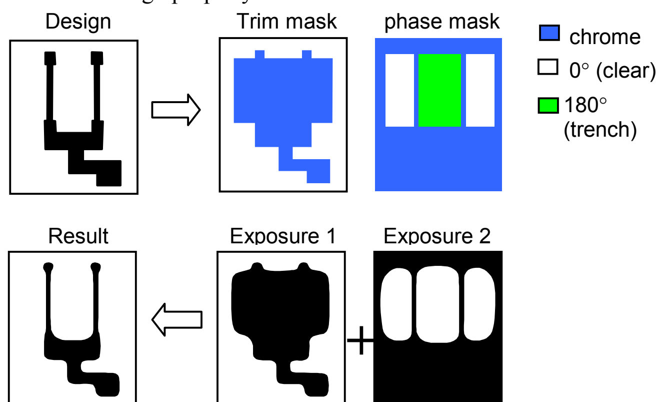

Figure 5: Gate shrink PSM lithography.

Figure 5 illustrates a double exposure PSM "gate shrink" methodology where the phase mask images transistor gate regions, and a trim mask images the remaining non-critical features [7]. Both masks require pattern-dependent layouts that can be generated with automated tools from several commercial vendors. In our experience, the rate at which cyclic conflicts occur depends heavily on design style. For the same design rule we see conflicts arise consistently in designs from some companies, while designs from other companies are completely free of conflicts.

2.1 IDEAL Imaging System

After a decade of mask process and equipment investment, production-worthy phase shift masks are now possible. However PSMs cost at least three times more than conventional masks. One way to reduce the expense of PSMs is to reuse them on many designs. The IDEAL imaging system [8] developed by Canon Inc. employs a reusable phase mask configured with an array of periodic lines in a first exposure (see Figure 6), and a conventional mask defining the specific circuit pattern in a second exposure. The conventional mask has clear regions, opaque regions, and partially transmitting regions made by a half tone pattern. The PSM mask is imaged as a fine grating pattern of 0-1 intensity levels, and the conventional mask is imaged at 0-1-2 intensity levels. Possible combined exposure levels are therefore 0-1-2-3. The example in Figure 6 shows how the heavy outlined figures in the combined exposure are achieved when the imaging threshold is set to print exposure levels of 2 or greater.

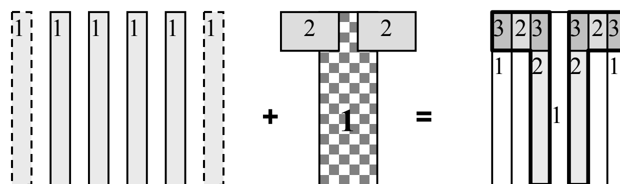

Figure 6: Principle of IDEAL imaging

IDEAL imposes two constraints on the design layout: 1) all critical lines must be oriented along one axis; 2) critical feature placements are constrained to an absolute grid across the chip.

2.2 GRATEFUL imaging system

GRATEFUL is a three-exposure PSM technique similar to IDEAL. A phase grating mask and a trim mask are used to define critical features, and a double resist exposure and process is used to define the interconnect features [9]. Because critical feature dimensions are defined solely by the phase grating exposure, it is claimed that OPC won't needed. GRATEFUL design layout constraints are the similar to those for IDEAL.

2.3 Phase Phirst imaging system

The proposed Phase Phirst methodology involves prefabricated mask blanks with standardized phase shift structure patterns underneath chrome and resist layers [10]. One anticipated advantage of Phase Phirst is lowered phase mask cost by virtue of mass production. Another advantage is its use of rugged sidewall chrome alternating aperture structures which have good imaging characteristics [11]. The proposal envisions a set of standard phase mask configurations to enable low-cost gate shrink PSM for common ASIC designs. Three possible phase layouts are shown in the top row of Figure 7. The layout design must ensure that all critical feature placements are aligned to phase boundary locations pre-established in the phase mask.

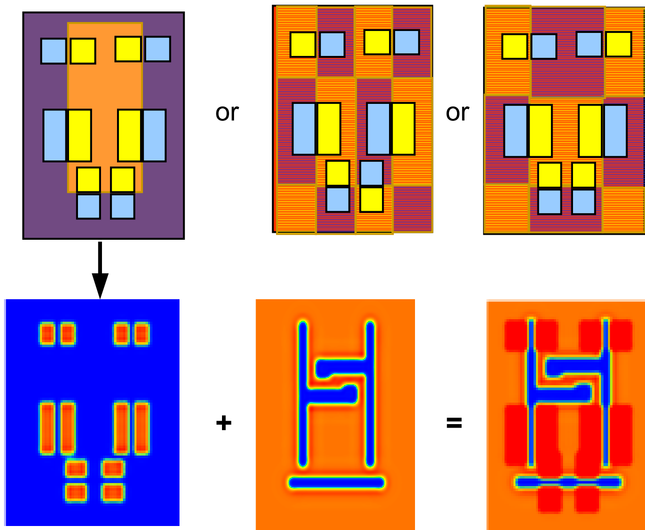

Figure 7: Use of Phase Phirst prefabricated phase mask blanks

2.4 Weak PSM imaging

Attenuated (weak) PSM is widely used for printing contact layers. Attenuated masks use partially transmitting, phase-shifted regions instead of opaque chrome to define dark areas. The mild phase effect between the background and main features sharpens contact images, improves depth of focus, and produces somewhat smaller, more uniformly sized vias on the wafer. At 5 to 10% of the clear intensity, the light transmitted by the attenuated areas is insufficient, by itself, to expose resist. However *sidelobes* – dim rings of light surrounding imaged bright features – can constructively interfere with each other to print unwanted features as shown in Figure 8. The key to preventing these artifacts is to ensure that design figures are arranged so that their sidelobes cannot harmfully contribute at common locations. The range of such optical interactions can extend several feature widths, therefore geometric rules alone may be insufficient to ensure artifact-free configurations. Fast optical simulation can provide a robust way to detect sidelobe-printing problems in arbitrary layout configurations.

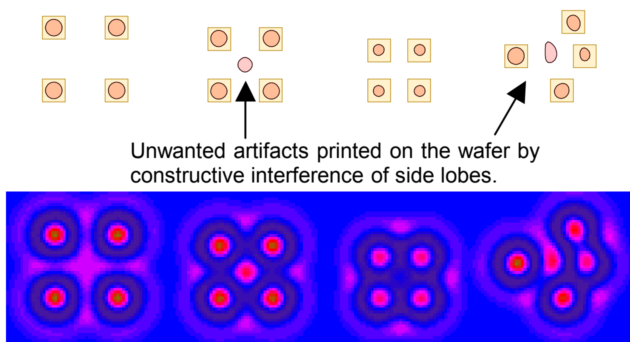

Figure 8: Optical simulation of attenuated mask contact patterns reveals unwanted artifacts.

3. Off-axis lithography and assist features

Off-axis illumination techniques are used to enhance the resolution of tightly pitched line patterns [12]. The so called dipole off-axis method is particularly interesting because it shows similar characteristics to alternating PSM. A layman's explanation is illustrated in Figure 9.

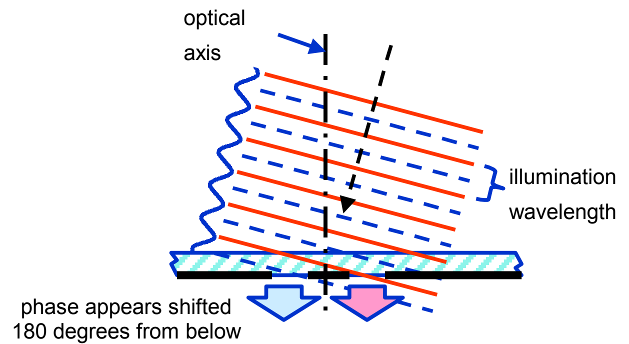

Figure 9: Off-axis lithography has characteristics similar to alternating PSM.

When a conventional mask is illuminated at an oblique angle (tilted from the optical axis) the phase of the light front varies along the mask. At a particular mask aperture spacing, determined by the off-axis angle and the wavelength, the light seen by the lens will alternate phase between 0 and 180 degrees, thus imitating the behavior of alternating phase masks. A dipole off-axis simulation of line space patterns in Figure 10 shows that dense lines at the optimum pitch image well, isolated lines resolve. However, critical lines at certain space widths, or *dead zones*, won't print and must be avoided in the design layout. The only reliable way to determine whether arbitrary feature configurations will print is to simulate them with an off-axis optical model.

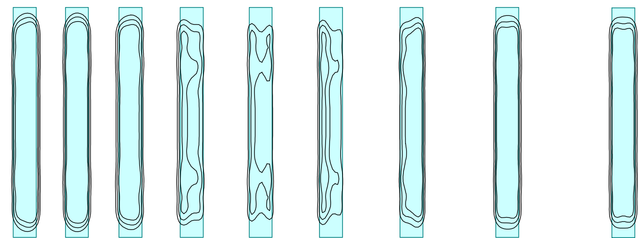

Figure 10: Simulation of line-space pattern with dipole off-axis illumination.

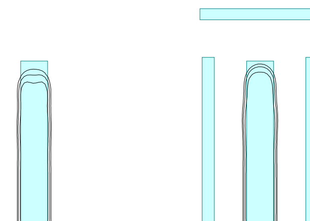

Figure 11: Assist features reduce shape variations due to varying focus conditions.

Assist features are small lines placed on the mask to enhance the images of adjacent figures. The assist features themselves must be smaller than the resolving limit of the optics so they don't print on the wafer. The simulation in Figure 11 shows assist feature enhancements applied to an isolated line and its endpoint imaged with off-axis illumination. The main benefit is that the line shape is more resistant to process variations, represented by the focus window contours in Figure 11. The assist features also reduce line-end shortening. CD variations caused by proximity effects can be reduced with assist features, however we see a general

preference to apply OPC on main features in conjunction with assist feature use.

Optimum placement of assist features depends on the shape and width of the associated critical feature and the spacing between structures. Layout designs are ideally constrained to avoid space widths that preclude or limit the placement of assist features as shown in Figure 12.

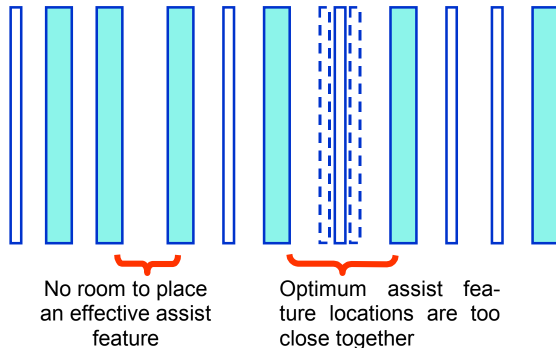

Figure 12: Layout space widths to avoid for assist feature use.

The ideal layout for assist feature treatment constrains each critical feature placement so that its neighbors are exactly one, two, or at least three critical pitch widths away.

4. OPC and RET

With the possible exception of GRATEFUL, none of the resolution enhancement techniques discussed here eliminate proximity effects. The need for aggressive OPC will increase, working in conjunction with RET.

In our experience we've found that some layout configurations are less "correctable" than others. The overall goal of OPC is to restore dimensional accuracy while maintaining resistance to process variations. An OPC-unfriendly configuration is where there is no good compromise between these two objectives. For example "hidden corrections" are sometimes embedded in the design layout, such as line-end extensions where the intended line end is actually short of the drawn line. Without additional information to define the true OPC target configuration, OPC will unnecessarily correct wafer features to drawn dimensions and, in some cases, this will result in poor process variation behavior.

5. Conclusions

We have discusses a number of current and anticipated optical lithography techniques that impose new constraints on physical layout design. Assist features, off-axis illumination, and OPC are widely deployed in production today for DRAM, standard ICs, and ASICs. Aggressive assist feature and model-base OPC is under development at advanced fabs for 0.10µm production. Alternating PSM (gate shrink) technology is in development or pilot production primarily at DRAM and other high-volume standard IC manufacturers. A key barrier to deploying alternating PSM for low volume production (ASICs) is its higher mask cost. We believe ASIC foundries will more likely adopt lower cost PSM variations such as IDEAL or Phase Phirst for sub 0.1µm nodes.

RET compliance will affect library cell layouts, automated place and route tools, and verification. We believe the primary need today is to provide designers a tool set to verify existing designs for RET compliance, and to this end we have integrated RET synthesis -- including PSM phase and trim mask generation, assist feature generation, OPC, and wafer process simulation -- into our verification tool kit. A complete compliance check applies a virtual fabrication cycle to the design layout by executing anticipated RET/OPC treatments and simulating the output (mask layout) with calibrated wafer process models to predict what would be achieved on the wafer. Automated analyses of the simulation, with user-defined tolerances, pinpoint compliance problem areas [13]. We are also integrating RET-compliant synthesis algorithms into our automated physical layout tools.

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