An Upper Bound for 3D Slicing Floorplans

Silke Salewski, Erich Barke
Institute of Microelectronic Circuits and Systems, University of Hannover, Germany
{salewski,barke}@ims.uni-hannover.de

Abstract

As the impact of interconnect on IC performance and chiparea in deep submicron design increases, research activities on technologies for three-dimensional integrated circuits intensify. Nevertheless, there is not much work done on the automation of 3D-layout design. In this paper we survey slicing structures for 3D floorplans. We present an upper bound for the volume of such floorplans, which shows the usability of slicing structures for three-dimensional floorplanning.

1. Introduction

In recent years the investigation of the third dimension in IC design attracts growing attention due to several reasons. One of the most important ones is the increasing influence of the interconnect delays on IC performance and the fact that the wiring length can be evidently reduced by 3D technology [1, 2, 3, 4]. There are several proposed applications for three-dimensional ICs [5, 6, 7, 8, 9, 10, 11] and much research effort has been carried out on the new technologies for vertically integrated circuits. Beside the stacking of Multi-Chip-Modules (MCMs) [12], there exist several basic approaches to vertically connect multiple silicon layers [13, 14, 15, 16, 17].

Floorplanning plays a very important role in three-dimensional circuit design, since heat distribution on the chip gets a crucial factor [18, 19, 4] and should be accurately planned in an early phase of the physical design. Moreover, the growing size of the circuits enforce the necessity to stack and interconnect several silicon layers and therefore will make common placers obsolete.

In the two-dimensional case slicing floorplans [20, 21] have proved to produce good results [22, 23]. Therefore, we study the facilities of slicing structures for general three-dimensional floorplans. Those floorplans will be capable of handling vertically stacked ICs (two and a half dimensional) as well as complete three-dimensional chip technologies that might come up in the future.

The remainder of this paper is organized as follows. In Section 2 we will review previous work on mathematical estimation of slicing floorplans. In Section 3 we introduce the problem and some notation. We present our main result in Section 4 and give some concluding remarks and an outlook to future work in Section 5.

2. Previous work

Slicing floorplans in 3D are not explored yet, but there was much research on slicing floorplans in 2D. Young and Wong proposed an upper bound for the area of such floorplans in [24]. They showed that this bound is given by the following formula:

$$area(F) \le \min\left\{(1+\frac{1}{\lfloor\sqrt{r}\rfloor}), \frac{5}{4}, (1+\alpha)\right\} A_{total}\text{, where}$$

$$\alpha = \sqrt{\frac{2A_{max}}{rA_{total}}}\text{, } A_{total} = \sum_{i=1}^{n} A_i\text{, } A_{max} = \max_{1\le i\le n}\{A_i\}$$

and the shape flexibility $r \ge 2$. In [25] this bound was even improved. Both papers followed the same idea for their proof. They used a special constructive packing algorithm to obtain a slicing floorplan that is at most as large as the given bound. Therefore, they could show that at least one floorplan exists, which fulfills the proposed bounds. In our paper, we will follow this idea and modify the algorithm for the three-dimensional case.

3. Problem statement

A slicing floorplan in 3D is one that can be obtained by recursively dividing a cuboid with a plane in two parts. In our 3D floorplan problem we have to pack n modules of given volume V_i (*i=1..n*) tightly, so that the resulting volume of the enclosing cuboid is minimized.

Each module is represented by a cuboid C. We use $V(C)$, $h(C)$, $w(C)$ and $d(C)$ to denote the volume, the height, the width and the depth of C respectively. A soft cuboid is one that can change its shape while its volume is fixed. The shape flexibility of a soft cuboid specifies (analogical to the definition in 2D) the range of the aspect ratios of the height, width and depth respectively.

Therefore, we define, that a soft cuboid is said to have shape flexibility r, if C can be represented as any cuboid of given volume that meets all of the following three conditions:

$$\frac{1}{r} \le \frac{w(C)}{h(C)} \le r\ ,\quad \frac{1}{r} \le \frac{d(C)}{h(C)} \le r\ ,\quad \frac{1}{r} \le \frac{w(C)}{d(C)} \le r\ .$$

Equivalently the shape flexibility can be defined by the following single condition:

$$\frac{\max\left(w(C), d(C), h(C)\right)}{\min\left(w(C), d(C), h(C)\right)} \le r\ .$$

In this paper we give an upper bound for the volume of the optimal slicing floorplan, defined by the volume of the enclosing cuboid, if all the modules have shape flexibility of at least 2.

4. Main results

Theorem Given a set of soft modules each having shape flexibility $r \ge 2$ there exists a slicing floorplan F of these cuboids so that

$$V(F) \le \min\left\{1 + \frac{1}{\left\lfloor \sqrt[3]{r} \right\rfloor}, \frac{3}{2}, 1 + \alpha\right\} \cdot V_{total}$$

$$\text{with } \alpha = \left(\frac{2}{r}\right)^{2/3} \cdot \left(\frac{V_{max}}{V_{total}}\right)^{1/3}$$

$$\text{where } V_{total} = \sum_{i=1}^{n} V_i \quad \text{and} \quad V_{max} = \max_{1 \le i \le n}\left\{V_i\right\}\ .$$

This theorem follows directly from Lemma 1, Lemma 2 and Lemma 3 that are presented in the following. Note, that Lemma 1 is valid only for $r \ge 8$, but for $2 \le r < 8$ the first term is $1 + \frac{1}{\left\lfloor \sqrt[3]{r} \right\rfloor} > \frac{3}{2}$ and therefore the theorem still holds.

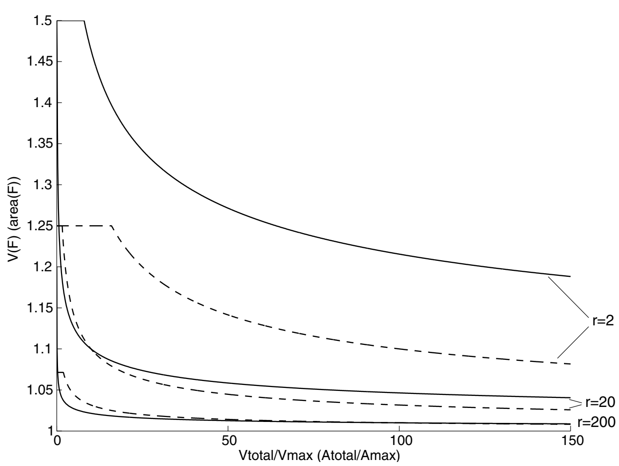

Figure 1. The upper bound of slicing floorplans in 3D (solid line) and 2D (dashed line).

Figure 1 shows the result in comparison with the upper bounds of the 2D case that is given in [24]. As expected, the dead space is larger in the three-dimensional case in most regions. But for large values of the shape flexibility r and the ratio A_{max} / A_{total} the difference is negligible. Remarkably, there exist even regions where the bound is lower in the three-dimensional case.

4.1. A bound for high shape flexibility

Lemma 1 Given a set of soft modules with each having shape flexibility $r \ge 8$ there exists a slicing floorplan F of these cuboids so that

$$V(F) \le \left(1 + \frac{1}{\left\lfloor \sqrt[3]{r} \right\rfloor}\right) \cdot V_{total}\ .$$

Proof We think of the optimal floorplan to be a cube of volume V_{total}. Therefore, the final floorplan is assumed to have a base area of $V_{total}^{1/3} \cdot V_{total}^{1/3} = V_{total}^{2/3}$. W.l.o.g. we assume $V_{total} = 1$. Thus, all values are dimensionless in the following. Moreover, we suppose the shape flexibility r to be a perfect cubic number. If it is not, we take r as the next lower number that is perfect cubic.

We divide the modules into groups depending on their volume. The packing algorithm sizes the cuboids, so that all modules of the same group have the same width and depth. The classification of the groups with the volume, the corresponding base area and height of the modules is given in Table 1.

Table 1. Classification of volumes in Lemma 1.

Group	Volume V	Base Area Q	Height H
1	$\frac{1}{r} \le V \le 1$	1	$\frac{1}{r} \le H \le 1$
2	$\frac{1}{r^2} \le V < \frac{1}{r}$	$\frac{1}{r^{\frac{2}{3}}}$	$\frac{1}{r^{\frac{4}{3}}} \le H < \frac{1}{r^{\frac{1}{3}}}$
3	$\frac{1}{r^3} \le V < \frac{1}{r^2}$	$\frac{1}{r^{\frac{4}{3}}}$	$\frac{1}{r^{\frac{5}{3}}} \le H < \frac{1}{r^{\frac{2}{3}}}$
⋮	⋮	⋮	⋮
i	$\frac{1}{r^i} \le V < \frac{1}{r^{i-1}}$	$\frac{1}{r^{\frac{2}{3}(i-1)}}$	$\frac{1}{r^{\frac{1}{3}(i+2)}} \le H < \frac{1}{r^{\frac{1}{3}(i-1)}}$
⋮	⋮	⋮	⋮

A cuboid C_i representing a module that belongs to Group i therefore has a volume $\frac{1}{r^i} \le V < \frac{1}{r^{i-1}}$ and a base area $\frac{1}{r^{\frac{2}{3}(i-1)}}$ and a height $H = V \cdot r^{\frac{2}{3}(i-1)}$. The shape flexibility condition is kept since

$$\max\left(w(C_i), d(C_i), h(C_i)\right) = \frac{1}{r^{\frac{1}{3}(i-1)}},$$

$$\min\left(w(C_i), d(C_i), h(C_i)\right) \geq \frac{1}{r^{\frac{1}{3}(i+2)}}, \text{ and thus}$$

$$\frac{\max\left(w(C_i), d(C_i), h(C_i)\right)}{\min\left(w(C_i), d(C_i), h(C_i)\right)} \leq r.$$

Now we place the modules one at a time from the largest to the smallest. We place each cuboid at the lowest possible level and then move it to the hindmost and leftmost position on that level. Because both, the width and the depth of the modules, decrease by $\sqrt[3]{r}$ from one group to another, it is always possible to place a cuboid in the described way and, moreover, the only wasted area appears at the irregular upper boundary. Now consider the uppermost cuboid C_{up}. Its lower boundary must be on a level less than the unit level, because otherwise $V_{total} > 1$. A module from Group 1 produces no dead space, thus the dead space size is upper bounded by $\frac{1}{\sqrt[3]{r}}$, because this is at most equal to the height of C_{up} and therefore the maximum height above the unit level, which gives us an upper bound on the volume. When r is not a perfect cubic number, then the upper bound is $\frac{1}{\left\lfloor \sqrt[3]{r} \right\rfloor}$, respectively.

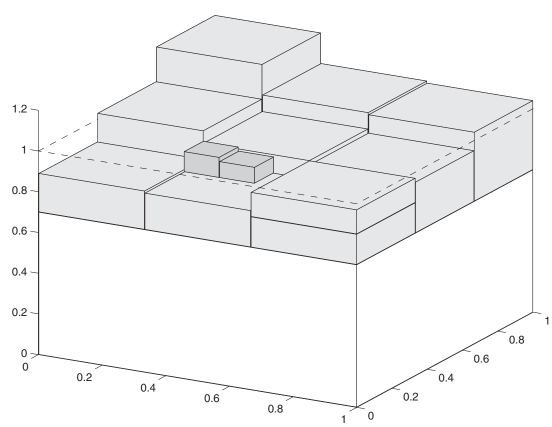

Figure 2. Example of a floorplan with $\left\lfloor \sqrt[3]{r} \right\rfloor = 3$ in Lemma 1. Cuboids of the same color belong to the same group, the dashed line indicates the unit level.

Figure 2 shows an example of a floorplan that is obtained by this packing algorithm. One can easily see that the resulting floorplan is slicing. □

4.2. A general upper bound

Lemma 2 Given a set of soft modules with each having a shape flexibility $r \geq 2$ there exists a floorplan F of these cuboids so that $V(F) \leq \frac{3}{2} \cdot V_{total}$.

Proof As before, we assume $V_{total} = 1$ and divide the cuboids in groups depending on their volume and use fixed base areas for packing them. However, we decrease the base area by a constant factor of 2. In order to ensure, that the cuboids fit in the base area of the complete floorplan and that the flexibility constraint is not violated, we have to do this as shown in Figure 3. Therefore, we can divide the modules into groups as given in Table 2.

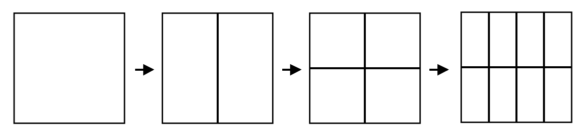

Figure 3. Base area reduction in Lemma 2.

The upper bound 1/2 for the dead space cannot be directly obtained from the heights of the modules in this case. Consider the uppermost cuboid C_{up}. Let $(1-x) \cdot w \cdot d \cdot h$ be the part of it that is above the unit level, with $x < 1$. A comparison of the striped and the dotted volume in Figure 4 leads to $(1-x) \cdot w \cdot d \cdot h \leq (1 - w \cdot d) \cdot x \cdot h$. Thus, it follows $w \cdot d \leq x$. Therefore, $B = (1 - w \cdot d) \cdot h$ is an upper bound for the dead space.

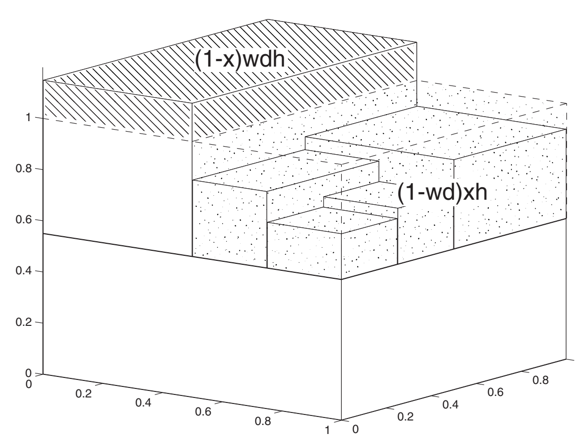

Figure 4. An example of a floorplan in Lemma 2.

Table 2. Classification of volumes in Lemma 2.

Group	Volume V	Base Area Q = Width W · Depth D	Height H	Bound $B = (1-Q)\cdot H$
1	$\frac{1}{2} \le V \le 1$	$1 = 1 \cdot 1$	$\frac{1}{2} \le H \le 1$	$B = 0$
2	$\frac{1}{4} \le V < \frac{1}{2}$	$\frac{1}{2} = \frac{1}{2} \cdot 1$	$\frac{1}{2} \le H < 1$	$B < \frac{1}{2}$
3	$\frac{1}{16} \le V < \frac{1}{4}$	$\frac{1}{4} = \frac{1}{2} \cdot \frac{1}{2}$	$\frac{1}{4} \le H < 1$	$B < \frac{3}{4}$
4	$\frac{1}{32} \le V < \frac{1}{16}$	$\frac{1}{8} = \frac{1}{4} \cdot \frac{1}{2}$	$\frac{1}{4} \le H < \frac{1}{2}$	$B < \frac{7}{16} < \frac{1}{2}$
5	$\frac{1}{128} \le V < \frac{1}{32}$	$\frac{1}{16} = \frac{1}{4} \cdot \frac{1}{4}$	$\frac{1}{8} \le H < \frac{1}{2}$	$B < \frac{15}{32} < \frac{1}{2}$
6	$\frac{1}{256} \le V < \frac{1}{128}$	$\frac{1}{32} = \frac{1}{8} \cdot \frac{1}{4}$	$\frac{1}{8} \le H < \frac{1}{4}$	$B < \frac{31}{128} < \frac{1}{4}$
7	$\frac{1}{1024} \le V < \frac{1}{256}$	$\frac{1}{64} = \frac{1}{8} \cdot \frac{1}{8}$	$\frac{1}{16} \le H < \frac{1}{4}$	$B < \frac{63}{256} < \frac{1}{4}$
⋮	⋮	⋮	⋮	⋮

From Table 2 we obtain, that only cuboids from group 3 can cause a dead space of more than 1/2. So consider C_{up} to be a cuboid of Group 3 with volume $\frac{1}{16} \le V(C_{up}) < \frac{1}{4}$. If $V(C_{up}) \le \frac{1}{8}$, then the height of C_{up} is $h(C_{up}) \le \frac{1}{2}$ and our bound is not exceeded. Therefore we assume $\frac{1}{8} < V(C_{up}) < \frac{1}{4}$.

Survey of two cases:

Case I: Besides C_{up} there are cuboids with a total base area of at least 1/2, which are above the unit level. Let $(1-x)\cdot w \cdot d \cdot h$ be the part of $V(C_{up})$ that is above the unit level, with $x < 1$. We obtain $(1-x)\cdot \frac{1}{4} \cdot h \le x \cdot h \cdot \frac{1}{4}$ by following the same argumentation that leads to the bound B and considering all modules above the unit level. Thus it follows $x \ge \frac{1}{2}$. Therefore, $(1-x)\cdot h \le \frac{1}{2}$ is an upper bound for the total dead space in this case.

Case II: Besides C_{up} there is less than a total base area of ½ above the unit level.

Subcase (i): Among the other cuboids, which are above the unit level, there is no other one of Group 3. Then we can move all these cuboids to the right half of the total floorplan and extend C_{up} to a depth of $d = 4 \cdot V(C_{up})$ while keeping $w = \frac{1}{2}$. Then $h(C_{up}) = \frac{1}{2}$ and our upper bound is not exceeded. From $\frac{1}{8} < V(C_{up}) < \frac{1}{4}$ it follows $\frac{1}{2} < d < 1$. Thus the flexibility constraints are not violated. Since the other cuboids are from other groups, the bound is not exceeded by them either.

Subcase (ii): Among the other cuboids above the unit level there is another cuboid C’ from Group 3. Figure 5 shows an example. Let h’ be its height and $(1-x)\cdot h' \cdot w' \cdot q'$ be the part of it above the unit level. Then $(1-x)\cdot h' \cdot \frac{1}{4} \cdot 2 \le x \cdot h' \cdot \frac{1}{2}$. It follows that $x \ge \frac{1}{2}$ and thus $(1-x)\cdot h' \le \frac{1}{2}$. Therefore, we can pack the cuboid C_{up} as in subcase (i) and neither the cuboid C’ nor the C_{up} will exceed the upper bound of 1/2 for the dead space. □

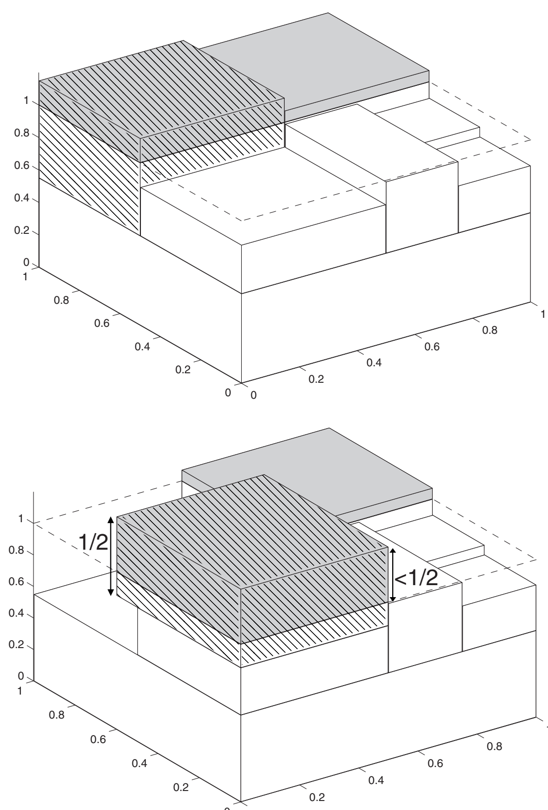

Figure 5. Post-processing of the striped cuboid C_{up} in Case II (ii) of Lemma 2.

4.3. An upper bound considering the relative sizes of the volumes

Lemma 3 Given a set of soft modules with each having a shape flexibility r≥2 there exists a floorplan F of these cuboids so that

$$V(F) \le \left\{ 1 + \left(\frac{2}{r}\right)^{2/3} \cdot \left(\frac{V_{max}}{V_{total}}\right)^{1/3} \right\} \cdot V_{total}\,.$$

Proof As before, we assume $V_{total} = 1$ and divide the modules into groups depending on their volume. In this case we take the size of the largest module into account for defining the base area x^2 of the cuboids of Group 1. Then the base area is halved from group to group in the same way as described in Lemma 2. An example of a floorplan, which is obtained in this way, is shown in Figure 6. The classification of the groups is given in Table 3.

Table 3. Classification of volumes in Lemma 3.

Group	Volume V	Base Area Q	Height H
1	$\frac{x^3}{r} \le V \le V_{max}$	x^2	$\frac{x}{r} \le H \le \frac{V_{max}}{x^2}$
2	$\frac{x^3}{2r} \le V < \frac{x^3}{r}$	$\frac{x^2}{2}$	$\frac{x}{r} \le H < 2 \cdot \frac{x}{r}$
3	$\frac{x^3}{8r} \le V < \frac{x^3}{2r}$	$\frac{x^2}{4}$	$\frac{x}{2r} \le H < 2 \cdot \frac{x}{r}$
4	$\frac{x^3}{16r} \le V < \frac{x^3}{8r}$	$\frac{x^2}{8}$	$\frac{x}{2r} \le H < \frac{x}{r}$
5	$\frac{x^3}{64r} \le V < \frac{x^3}{16r}$	$\frac{x^2}{16}$	$\frac{x}{4r} \le H < \frac{x}{r}$
6	$\frac{x^3}{128r} \le V < \frac{x^3}{64r}$	$\frac{x^2}{32}$	$\frac{x}{4r} \le H < \frac{x}{2r}$
⋮	⋮	⋮	⋮

If we use $x = \left(\frac{V_{max} \cdot r}{2}\right)^{1/3}$ then the height of all modules is $H \le \frac{V_{max}}{x^2} = 2 \cdot \frac{x}{r} = \left(\frac{2}{r}\right)^{2/3} \cdot V_{max}^{1/3}$. One can easily see that the flexibility constraint is not violated, since $\frac{4}{r} \le r$ for all $r \ge 2$. As before, the lower boundary of the uppermost cuboid C_{up} has to be below the unit level and thus its height gives an upper bound on the total height. The dead space can be obtained from $\Delta V(F) \le h(C_{up}) \cdot X$ with the base area of the total floorplan $X = x^2 \cdot \left(\left\lceil \frac{\sqrt[3]{V_{total}}}{x} \right\rceil\right)^2$. Thus the dead space is upper bounded by

$$\Delta V(F) \;\le\; h(C_{up}) \cdot X \;\le\; 2 \cdot \frac{x}{r} \cdot x^2 \cdot \left(\left\lceil \frac{\sqrt[3]{V_{total}}}{x} \right\rceil\right)^2$$

$$\Delta V(F) \le\; 2 \cdot \frac{x}{r} \cdot V_{total}^{2/3} \;=\; \left(\frac{2}{r}\right)^{2/3} \cdot \left(\frac{V_{max}}{V_{total}}\right)^{1/3} \cdot V_{total}\,. \quad \square$$

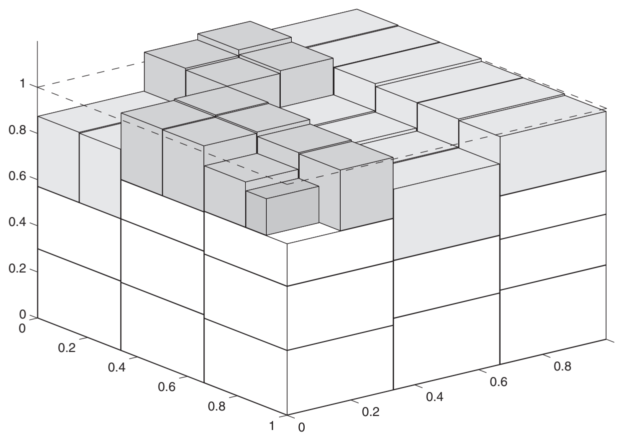

Figure 6. An example of a floorplan in Lemma 3. Cuboids of the same group are illustrated in the same color.

5. Conclusion and future work

In this paper we gave an upper bound for the volume of 3D slicing floorplans. The proposed bound shows that slicing structures are well suited for investigating the third dimension in floorplanning. In three-dimensional layout design it is important to reserve space for routing, since basically there are no special routing layers. Therefore, even the bound of 3/2 is an admissible value. Moreover, this is only an upper bound, and we expect to obtain a much lower value in the average case, as it is the case in two dimensions [24]. Therefore, we will implement an algorithm for 3D slicing floorplans to compare the theoretical bound given in this paper with the average case of an actual implementation.

References

[1] R. Zhang, K. Roy, C.K. Koh, D.B. Janes, “Stochastic Interconnect Modeling, Power Trends, and Performance Characterization of 3-D Circuits”, *IEEE Transactions on Electron Devices*, Vol. 48, No.4, 2001, pp. 638-652.

[2] S.J. Souri, K. Banerjee, A. Mehrotra, K.C. Saraswat, “Multiple Si Layer ICs: Motivation, Performance Analysis, and Design Implications”, *Proceedings of the Design Automation Conference 2000*, pp. 213-220.

[3] A. Rahman, A. Fan, J. Chung, R.Reif, “Wire-Length Distribution of Three-Dimensional Integrated Circuits”, *IEEE International Interconnect Technology Conference Proceedings*, 1999, pp. 233-235.

[4] K. Banerjee, S.J. Souri, P. Kapur, K.C. Saraswat, “3D-ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration”, *Proceedings of the IEEE*, Vol. 89, No.5, 2001, pp. 602-633.

[5] N. Takahashi, N. Senba, Y. Shimada, I. Morisaki, K. Tokuno, “Three-Dimensional Memory Module”, *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, Vol. 21, No. 1, 1998, pp. 15-19.

[6] T. Endoh, H. Sakuraba, K. Shinmei, F. Masuoka, “New Three Dimensional (3D) Memory Array Architecture For Future Ultra High Density DRAM”, *22nd International Conference on Microelectronics (MIEL 2000)*, Vol. 2, pp. 447-450.

[7] K.W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, H. Hasimoto, K.T. Park, H. Kurino, M. Koyanagi, “Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology”, *International Electron Devices Meeting 2000*, Techn. Digest, pp. 165-168.

[8] H. Kurino, K.W. Lee, T. Nakamura, K. Sakuma, K.T. Park, N. Miyakawa, H. Shimazutsu, K.Y. Kim, K. Inamura, M. Koyanagi, “Intelligent Image Sensor Chip with Three Dimensional Structure”, *International Electron Devices Meeting 1999*, Techn. Digest, pp. 879-882.

[9] J. Burns, L. McIlrath, C. Keast, C. Lewis, A. Loomis, K. Warner, P. Wyatt, “Three-Dimensional Integrated Circuits for Low-Power, High-Bandwith Systems on a Chip”, *IEEE International Solid-State Circuits Conference 2001*, pp. 268-269.

[10] M. Koyanagi, Y. Nakagawa, K.W. Lee, T. Nakamura, Y. Yamada, K. Inamura, K. Park, H. Kurino, “Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology”, *IEEE International Solid-State Circuits Conference 2001*, pp. 270-271.

[11] S. Chiricescu, M. Vai, “A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data”, *International Symposium on Circuits and Systems 1998*, Vol.2, pp. 232-235.

[12] S.F. Al-Sarawi, D. Abbott, P.D. Franzon, “A Review of 3-D Packaging Technology”, *IEEE Transactions on Components, Packaging, and Manufacturing technology-Part B*, Vol. 21, No.1, 1998, pp. 2-14.

[13] P. Ramm et. al., “Three Dimensional Metallization for Vertically Integrated Circuits”, *Microelectronic Engineering* 37/38 (1997), pp. 39-47.

[14] A. Fan, A. Rahman, R. Reif, “Copper Wafer Bonding”, *Electrochemical and Solid State Letters*, Vol. 2, No. 10, 1999, pp. 534-536.

[15] T. Kunio, K. Oyama, Y. Hayashi, M. Morimoto, “Three Dimensional ICs, having Four Stacked Active Device Layers”, *International Electron Devices Meeting 1989*, pp. 837-840.

[16] G.W. Neudeck, S. Pae, J.P. Denton, T. Su, “Multiple Layers of Silicon-on-Insulator for Nanostructure Devices”, *Journal of Vacuum Science and Technology B* 17(3), 1999, pp. 994-998.

[17] V. Subramanian, K.C. Saraswat, “High-Performance Germanium-Seeded Laterally Crystallized TFT's for Vertical Device Integration”, *IEEE Transactions on Electron Devices*, Vol 45, No. 9, 1998, pp. 1934-1939

[18] M.B. Klein, S.A. Kühn, P. Ramm, W. Weber, “Thermal Analysis of Vertically Integrated Circuits”, *International Electron Devices Meeting 1995*, Techn. Digest, pp. 487-490.

[19] S. Im, K. Banerjee, “Full Chip Thermal Analysis of Planar (2-D) and Vertically Integrated (3-D) High Performance ICs”, *International Electron Devices Meeting 2000*, Techn. Digest, pp.727-730.

[20] D.F. Wong, C.L. Liu, “A New Algorithm for Floorplan Design”, *Proceedings of the Design Automation Conference 1986*, pp.101-107.

[21] R.H.J.M. Otten, “Automatic Floorplan Design”, *Proceedings of the Design Automation Conference 1982*, pp. 261-267.

[22] R.H.J.M. Otten, “What is a Floorplan?”, *International Symposium on Physical Design 2000*, pp.212-217.

[23] M. Lai, D.F. Wong, “Slicing Tree Is a Complete Floorplan Representation”, *Design, Automation and Test in Europe 2001*, pp.228-232.

[24] F.Y. Young and D.F. Wong, “How Good are Slicing Floorplans?”, *International Symposium on Physical Design 1997*, pp. 144-149.

[25] H.P. Peixoto, M.F. Jacome, and A. Royo, “A Tight Area Upper Bound for Slicing Floorplans”, *XIII. International Conference on VLSI Design 2000*, pp. 280-285.