Low-Voltage Memories for Power-Aware Systems

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ABSTRACT
This paper describes low-voltage RAM designs for stand-alone and embedded memories in terms of signal-to-noise-ratio designs of RAM cells and subthreshold-current reduction. First, structures and areas of current DRAM and SRAM cells are discussed. Next, low-voltage peripheral circuits that have been proposed so far are reviewed with focus on subthreshold-current reduction, speed variation, on-chip voltage conversion, and testing. Finally, based on the above discussion, a perspective is given with emphasis on needs for high-speed simple non-volatile RAMs, new devices/circuits for reducing active-mode leakage currents, and memory-rich SOC architectures.

Keywords
subthreshold current, DRAM and SRAM cells, gain cells, peripheral circuits, gate-source/substrate-source back-biasing, multi-V_T, on-chip voltage converters, testing, non-volatile RAMs, memory-rich architectures.

1. INTRODUCTION
Stand-alone memories and embedded memories (e-memories) for a system-on-a-chip (SOC) [1] have rapidly evolved, and thereby both dramatically reduced costs and greatly improved the performance of PCs, workstations, and servers. Consequently, high-density stand-alone memories have achieved a 4-Gb DRAM [2], a 32-Mb SRAM, and a 1-Gb flash memory [3] at R&D level. The power dissipations have also decreased by reducing the standard power-supply voltage (V_{DD}) to as low as 1.8V to 3.3V. High-speed e-memories, which are forecast to occupy over 90% of a low-power SOC [4], have also rapidly developed, as exemplified by a 300-MHz 16-Mb DRAM macro [5], a 1-GHz 24-Mb L3-SRAM cache [6], and a 1.2-V-read 16-Mb flash memory [7]. To enable applicability in minimized-size devices the V_{DD} of e-memories has been reduced in accordance with the rapidly reducing V_{DD} of MPUs [8] to below 1.5V. Recently, however, in accordance with the rapidly-growing power-aware-systems market, lowering the V_{DD} has further accelerated reducing e-memory power. Such is the case even for stand-alone memories that are applied to a low-power system-in-a-package (SIP), which has rapidly become widely used. As the V_{DD} reaches sub-V levels, however, two design issues arise [9]: the high signal-to-noise-ratio (S/N) design for memory cells for stable operations; and reduction of the ever-increasing leakage(gate-tunnel/subthreshold) currents of MOSTs that are seen when reducing the gate-oxide thickness (t_{ox}) and the threshold voltage (V_T). In particular, reducing the leakage current is vital for all future LSIs. Thus, some high-k gate insulators have been intensively developed to reduce the tunnel current. Moreover, new devices such as fully-depleted (FD) SOI and the dynamic-V_T (DTMOST) [10] using a partially-depleted SOI have been developed to reduce the subthreshold current. However, the subthreshold swing (i.e., S-factor) of FD SOI is still larger and DTMOST limits the V_{DD} to be around 0.4V at the most due to a rapidly increased pn-junction forward current [11]. Thus, circuit solutions are vital.

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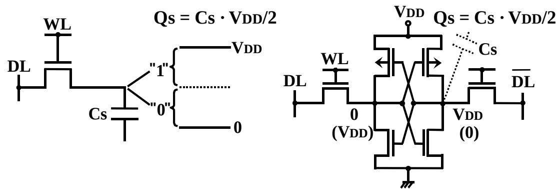
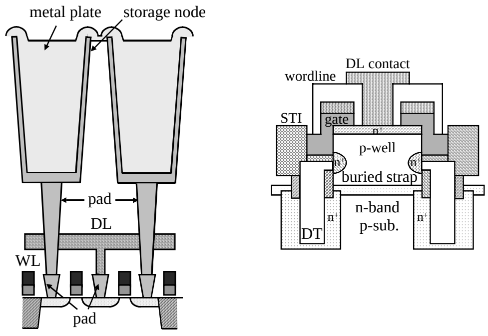


Figure 1 Memory-cell circuits of DRAM(a) and SRAM(b).

This paper mainly discusses low-voltage memory circuits, focusing on RAMs because they cover large parts of low-voltage flash-memory circuits. First, recent developments for DRAM and SRAM cells are discussed. Next, peripheral logic circuits are investigated, including other design issues for low-V_{DD} operations such as speed variations, on-chip supply-voltage converters, and a testing methodology. Finally, a perspective is given with emphasis on needs for non-volatile RAM cells, subthreshold-current reduction circuits for use in active mode, and memory-rich SOC architectures.

2. CURRENT RAM CELLS
The lower limit of the V_{DD} is determined by the S/N of the memory cell, the unscalable V_T of the memory-cell MOST, and the unscalable V_T -mismatch between cross-coupled/paired MOSTs in a large number of DRAM sense amps (SAs) and SRAM cells [9]. The S/N degrades at a lower V_{DD} because the signal charge ($Q_S = C_S V_{DD}/2$, C_S: storage capacitance) for DRAM and SRAM cells (Fig.1) decreases and thus causes a smaller signal voltage on the data line (DL) in a noisy memory array as well as larger soft errors. The unscalable V_T is a result of the specifications set to satisfy a required refresh time (t_{REFmax}) of the DRAM or the data-retention current of the SRAM. Both the V_T and the V_T -mismatch increase with increasing memory capacity and decreasing device size, while Q_S decreases [9].



(a) (b)

Figure 2 Stacked(a) and trench(b) capacitor DRAM cells[12, 41].

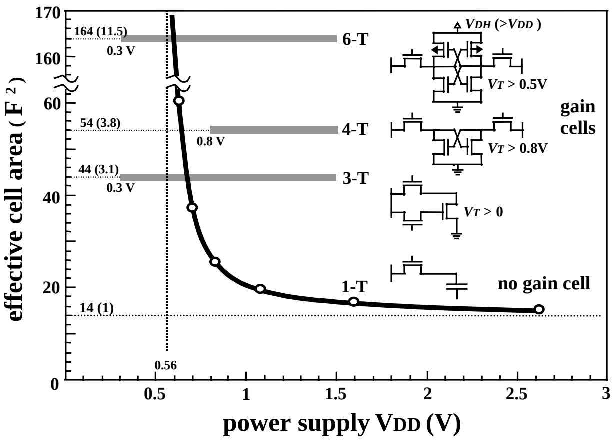


Figure 3 Effective cell area versus power supply[1, 8]. Non-self-aligned contact is used.

2.1 DRAM Cells

2.1.1 1-T Cells for Stand-Alone DRAMs

For a given cell-signal voltage ($\approx C_S V_{DD}/2C_D = Q_S/C_D$, C_D; DL-capacitance) of approximately 200mV read out on each DL, minimizing the cell size and the overhead areas for reducing the memory-chip size is the first priority for stand-alone DRAMs. It results in a large C_D because as many memory cells as possible are connected to each DL-pair to reduce the overhead area at each DL-division. A large Q_S (e.g., a large C_S) is thus needed for a necessary signal voltage, which has been realized by using sophisticated vertical(stacked/trench)-capacitors(Fig.2)and high-*k* thin-films. Relaxing the sophistication of the process/device requires reducing the C_S, which is realized by having a high V_{DD} and a smaller C_D through the multi-divided DL [9] using multi-level metal wiring. Applying self-aligned contact to memory cells only reduces the cell area despite a speed penalty being inflicted due to the increased contact resistance. A 6-4F^2 (F: feature size) trench-capacitor vertical-MOST cell[12,13] and a 6F^2 stacked-capacitor open-DL cell, in which array noise must be reduced by a low-impedance array [14], are leading developments of R&D. Even for such high-Q_S cell, however, the effective cell area, the sum of the genuine cell area and the overhead area at a DL-division, sharply increases with a decreasing V_{DD} [1,8] (Fig.3), because no gain of the 1-T cell requires more DL-divisions at a lower V_{DD} to maintain the necessary signal voltage.

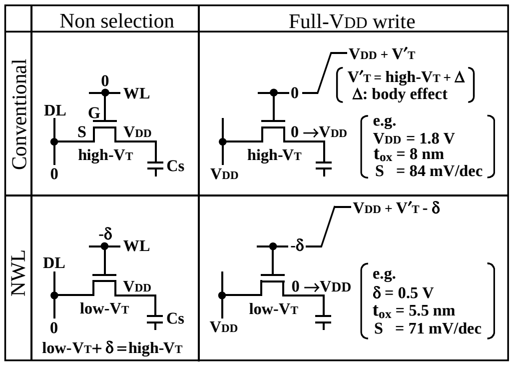
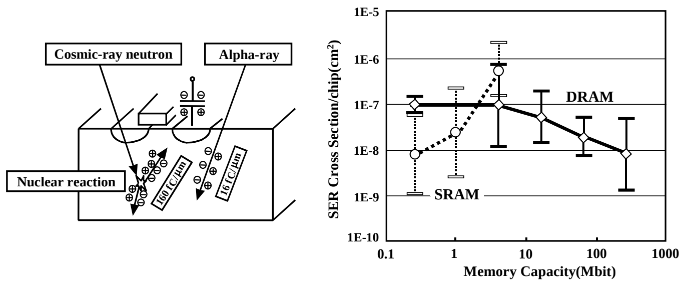


Figure 4 Conventional and negative word-line schemes[1].



(a) (b)

Figure 5 Mechanisms(a) and cross section(b) of soft errors[15].

Adjusting the potential profile of the storage node to suppress the *pn*-leakage current makes $t_{REF}max$ longer, and preserves the refresh busy rate even for larger memory-capacity DRAMs [9], or it lowers the data retention current in standby mode. The subthreshold current caused by the resultant low V_T is cut by the negative word-line (NWL) scheme (Fig.4) [9] with a δ gate-source back-bias during the non-selected period. Fortunately, reducing the word-line voltage by δ in a full-V_{DD} write-operation allows using a thinner-t_{ox} MOST for a given stress voltage, enabling a low-voltage operation with the resultant small *S*-factor. The DRAM cells are resistant against cosmic-ray neutron-hitting [15] (Fig.5), which generates about ten times as many charges as alpha particles. Soft errors gradually decrease with decreasing device size due to a rather large *Cs* and spatial scaling that reduces collection of charges generated by the hitting.

2.1.2 1-T Cells for e-DRAMs

Using a high-speed logic compatible process and a small sub-array are keys. Such a process is realized by using a non-self-aligned contact and a MOS-planer capacitor, as it was commonly done in the mid1970's. This is attractive as long as the resultant cell is quite a lot smaller than the 6-transistor (6-T) full CMOS SRAM cell [8]. A small sub-array allows even the resultant small C_S to develop enough signal voltage with an extremely low C_D that is realized by increasing the number of DL-divisions for a relatively high V_{DD} . The small sub-array also reduces array-relevant line delays that are major delays on the access/cycle path, achieving a high speed. A multi-bank interleaving with many small sub-arrays, pipeline operations, and direct sensing [9] solve the problem of the row-cycle of DRAM being slow, while enabling a faster access time than SRAM due to the smaller

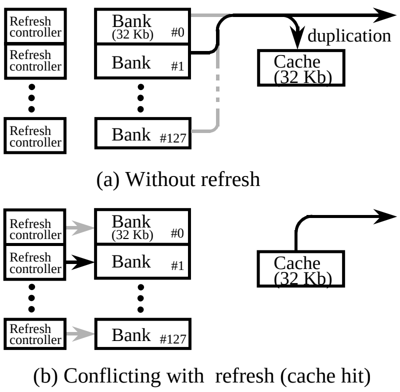


Figure 6 Read operations of multi banks of 1-T SRAM™[17].

physical size of the DRAM array for a given memory capacity. The small sub-array also allows the t_{REFmax} to be drastically shortened for a given junction temperature. It may even accept the open-DL cell, which is noisy but smaller than the traditional folded-DL cell, because the small sub-array causes little noise. Here, the soft-error issue that is unavoidably arisen due to a small C_S could be solved by using an error checking and correcting (ECC) circuit [16].

A good example is the so-called 1-T SRAM™ (Fig.6) [17], in which a 1-T DRAM cell with a C_S smaller than 10fF is realized by a single poly-Si planar capacitor and an extensive multi-bank scheme with 128 banks (32Kb in each) that are simultaneously operable is used. A row access frequency higher than 300-MHz was achieved for a 0.18-µm 1.8-V 2-Mb e-DRAM. A DRAM cache with the same capacity as a single bank is used to hide the refresh operation: Even when a conflict between a normal access and a refresh operation at the same bank arises, a cache hit occurs while permitting a refresh cycle for that bank since all of the data in that bank have been copied to the cache.

Low-voltage high-speed sensing is also essential. Although the standard mid-point (a half-V_{DD}) sensing [9] halves the DL power without a dummy cell, it slows down the sensing operation. In overdrive sensing [18,19] this problem is solved by applying a higher voltage solely to the SA-inputs with isolating the data line from the SA or with coupling capacitively. Using additional capacitors may be acceptable in e-DRAMs for which area is not a concern. Even full-V_{DD} (or ground) sensing with a dummy cell for a 1.5-V 16-Mb e-DRAM [5] was recently reported on, which is a revival of the sensing conducted in the NMOS DRAM era in 1970's.

2.1.3 Gain Cells

Gain cells would solve the above-mentioned problems of the 1-T cell, i.e., increasing the effective cell area at a lower V_{DD} and with sophisticated structures. The 3- and 4-transistor (3-T and 4-T) DRAM cells, and the 6-T SRAM cell, as shown in Fig.3, require no special capacitor. In addition, they are all gain cells that can develop a sufficient signal voltage without increasing the number of DL-divisions even at a lower V_{DD}, and thus provide a fixed effective cell area that is independent of the V_{DD}. Actually, however, the V_{DD} has a lower limit for each cell. For the 3-T cell, it would be around 0.3V if the V_T of the storage MOST is chosen to be around 0V. For the 4-T cell, it would be as high as 0.8V because the V_T of cross-coupled MOSTs must be higher than 0.8 V to ensure t_{REFmax} by eliminating the subthreshold current. For

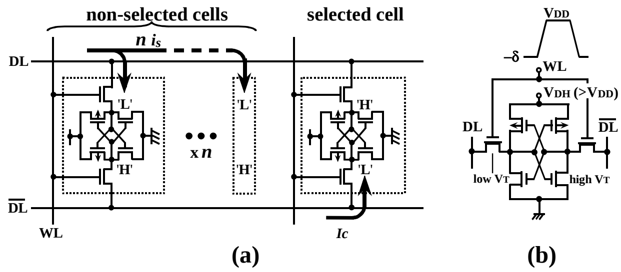


Figure 7 Data pattern of cells along the data line(a), and low-voltage SRAM cell(b)[9].

the 6-T SRAM cell, it would be around 0.3V if a raised supply voltage (V_{DH}) higher than 0.5V is supplied from an on-chip charge pump, as explained later. Consequently, the 3-T cell would be the smallest at less than 0.6-VV_{DD}. Recently, a small poly-Si vertical-transistor 2-T 5F^{2}gain cell [20] has been proposed despite a small current drivability of the transistor.

2.2 SRAM Cells

Reducing the cell area is the biggest concern regarding SRAMs, as an on-chip L3 cache shows [6]. The loadless CMOS 4-T SRAM [21] is attractive because the cell area is only 56% of that of the 6-T cell. However, it suffers from the data-pattern problem, which we discuss below, and difficulty in controlling the non-selected word-line voltage precisely to maintain the load current. At present, the 6-T cell is the best despite its large area because it enables a simple process and design provided by the cell's wide-voltage margin. Even for this cell, subthreshold currents increase the retention current with lowering the V_T, reaching as much as 10A even for a 1-Mb array for V_T = 0V [9]. This limits the reduction of V_T tightly. The voltage margin of the cell decreases with decreasing V_{DD} and V_T, and requires a decrease in the ratio of transconductance of the transfer MOST to that of the driver MOST. It further decreases if the V_T and V_T-mismatches between paired MOSTs vary, and if the V_T of the transfer MOST is low. A low-V_T transfer MOST may cause a read failure when the total subthreshold current from transfer MOSTs of multiple non-selected cells along DL is greater than the selected cell's current in the worst cell data pattern (Fig.7). A hierarchical DL scheme partly solves this problem by limiting the number of memory cells connected to DL [22]. Using a data equalizer to compensate for the current [23] is also effective, despite an occurring area penalty. Moreover, a gate-source offset-driving memory cell allows using a low-V_T transfer MOST for a high-speed and negligible DL current [24], although eleven transistors are required for each cell.

Eventually, a solution might be combining high-V_T cross-coupled MOSTs and a raised power supply, as shown in Fig.7 (b) [25], in terms of signal charge, subthreshold current, and V_T-imbalance immunity. Here, a low-V_T transfer MOST coupled with an NWL scheme achieves high speed while reducing the leakage currents from cells along DL. A similar concept incorporated for a 0.4-V-V_{DD} 0.18-µm 256-Kb SRAM [26] showed excellent performances of an active power of only 140 µW at 4.5 MHz and a standby current of 0.9µA at a substrate back-bias of 0.4V at $V_{DH} - V_{DD}$ = 0.1V and V_T = 0.4-0.5V. Even for the raised power supply, SRAM cells may inevitably require either an additional capacitor at the storage node [27] or the use of an ECC technique to prevent soft errors in the future. This is because the SRAM soft errors rapidly increase with device scaling (Fig.5), due to its small parasitic node capacitance.

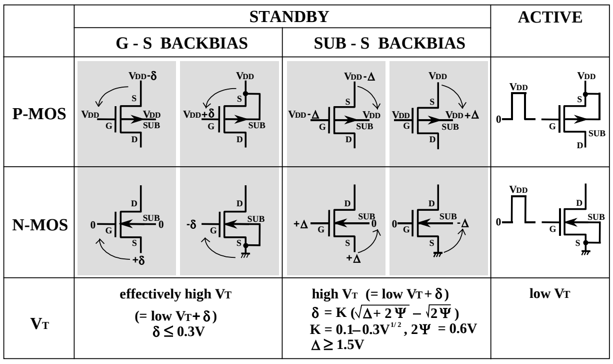


Figure 8 Dynamic-V_T schemes[9].

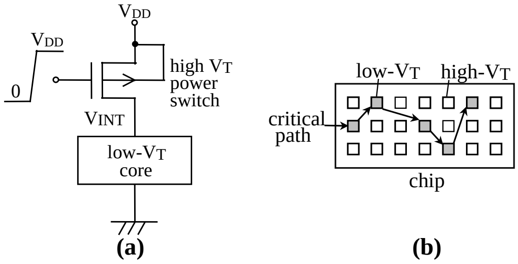


Figure 9 Power switch(a) and multi-V_T scheme[9].

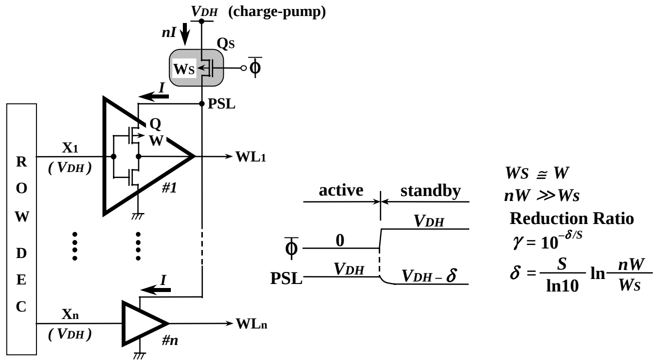


Figure 10 G-S backbias applied to DRAM word drivers[29, 30].

3. PERIPHERAL LOGIC CIRCUITS

3.1 Subthreshold-Current Reduction

Memory peripheral circuits favor subthreshold-current reduction [9]: They consist of multiple iterative circuit blocks, such as row/column decoders and drivers, each of which has quite a large total-channel width involving the subthreshold current, and all circuits in the block, except for a selected one, are inactive even during an active period, enabling simple and effective subthreshold-current control with a small area penalty, which is discussed later. In addition, a slow memory cycle allows each circuit to be active only for a short period within the "long" memory cycle, enabling additional time for the subthreshold-current control. Moreover, the circuits are input-predictable, enabling designers to predict all node voltages in a chip, and to prepare the subthreshold-current reduction scheme in advance.

Two reduction methods have been proposed. One method is the dynamic V_T scheme (Fig.8) [9]. The V_T is low enough to enable high speed in active mode due to no back-bias connection. In standby mode it is raised to reduce the subthreshold current by changing the bias condition. This is further categorized as gate-source (G-S) back-biasing and substrate-source (Sub-S) back-biasing. The other method is the static V_T scheme (Fig.9), which is categorized as a power-switch and multi-V_T scheme. Both methods are effective for standby mode. Even so, they are insufficient for active mode unless a high-speed reduction control necessary at active mode is achieved. In this sense, the Sub-S back-biasing and the power switch are not applicable to active mode because a large voltage swing is involved.

3.1.1 Standby Mode

G-S Back-Biasing: S-control with a fixed G, and G-control with a fixed S are well known. In this scheme, a small voltage swing (δ) suffices for the reduction and enables a high-speed recovery. Note that an effectively high V_T is established as the sum of a low-actual V_T and δ, and the subthreshold current is reduced to 1/10 with a V_T-increment of only 0.1V (i.e. S = 0.1V/decade at 100°C). In particular, S-control applied to iterative circuit blocks such as a word driver block is extremely important for memory designs. For example, a low-V_T PMOS switch [29, 30] (Qs in Fig.10) shared with n word drivers enables the common power line (PSL) to drop by δ as a result of the total subthreshold current flow of nI when the switch is off in standby mode. It provides each PMOS driver (Q) with a δ self-back-bias so the subthreshold current (I) eventually decreases. Hence, even if an on-chip charge pump for a raised supply V_{DH} necessary for the DRAM word-bootstrapping suffers from the poor output-current drivability, the V_{DH} is well regulated. In active mode the selected word line is driven after connecting the PSL to a supply voltage (V_{DH}) by turning on Q_S. Here, the Q_S-channel width can be reduced to an extent comparable to that of the Q-channel width without a speed penalty because only one of the n drivers is turned on. For a 256-Mb chip, a δ as little as 0.25V reduced the standby subthreshold-current by 2-3 decades without inflicting penalties in terms of speed and area. The S-control is also applicable to dynamic NAND decoders, which are common in memory, even without a level keeper [31]. Examples of G-control are the NWL scheme, as discussed before, G-S offset drive [9], and an application to a power switch, as explained later.

Sub-S Back-Biasing: Sub-control with a fixed S, and S-control with a fixed Sub are well known methods [9]. For a larger V_T-change (ΔV_T), a large Sub-swing or S-swing (i.e., $\Delta (V_{SUB} - V_S) = \Delta V_{BB}$) is needed. The swing, however, is quite large. For example, existing MOSTs with a 0.2-$V^{1/2}$ body constant require a 2.5-V ΔV_{BB} to reduce the current by 2 decades with a 0.2-V ΔV_T. A larger body-constant (K) MOST is also needed. However, it slows down the speed for stacked circuits such as a NAND gate. On the contrary, the K value decreases with MOST scaling, implying that the necessary ΔV_{BB} will increase further and further in the future due to a lower K and the need for a larger ΔV_T escalated at the low-V_T era. Eventually, this enhances short-channel effects and increases other leakage currents such as the gate-induced drain-lowering (GIDL) current [32]. A shallow reverse V_{BB} setting or even forward V_{BB} setting in active mode is also required because the V_T is more sensitive to the V_{BB} [9]. However, requirements for V_{BB}-noise suppression become more stringent instead. The connection between Sub and S every 200 μm [33] reduces the noise at the area penalty.

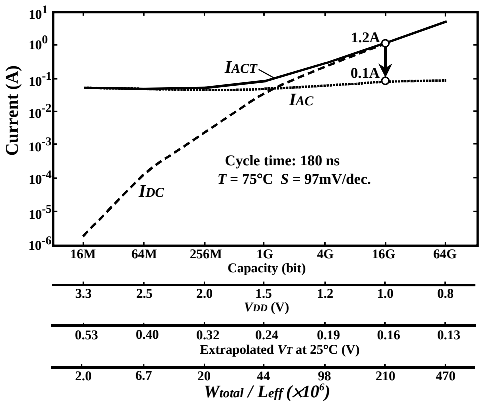


Figure 11 Trends in DRAM active current[28, 42].

Multi-Static V_T: Applying dual-V_T scheme [9] to the critical path of peripheral logic circuits is quite effective. A 0.1-V V_T -difference reduces the standby subthreshold current to one fifth of its value for a single low V_T , although a larger V_T -difference might cause a race problem between low- and high-V_T circuits. In a DRAM [9] multi-V_T can easily be produced by applying internal supply voltages (lowered and raised from V_{DD}) generated by on-chip voltage converters. A combination of dual V_T and dual V_{DD} has also been proposed for making a 1-V e-SRAM [34].

Power Switch: A high-V_T PMOST power switch [9], applied to a low-V_T internal core, completely cuts the subthreshold current from the core by turning off the switch in standby mode. The drawbacks are a large V_{DD} swing at the internal power line, causing a large power/spike current and slow recovery at mode transitions, and need for a large PMOST. Using a low-V_T instead reduces the size for a given transconductance, while the subthreshold current at standby mode is shut down if the G-control is applied.

3.1.2 Active Mode

In the future, with further reducing V_T , the subthreshold current (I_{DC}) will exceed the capacitive current (I_{AC}) and eventually dominate the total active current (I_{ACT}) of the chip (Fig.11), as pointed out as early as 1993 [28, 42]. Partial activation of a multi-divided iterative circuit block [9], coupled with G-S back-biasing, can confine subthreshold currents to a single selected sub-block. The above-mentioned multi-static V_T also reduces the currents. In fact, it has been reported that these circuits could reduce the active current of a hypothetical 16-Gb DRAM [28] from 1.2A to 0.1A (Fig.11), although the effectiveness with an actual chip has not been verified yet.

3.2 Other Low-Voltage Relevant Issues

The speed-variation rate for a given variation in design parameters increases by lowering the V_{DD}. Controlling the V_{SUB} and the internal V_{DD} [35] in accordance with the parameter variations reduces the speed variation. Controlling a reverse V_{SUB}, for example, reduced the variation of logic circuits by 20%. Controlling a forward V_{SUB} is more effective for reducing speed variations [36] because the V_T is more sensitive to the V_{SUB}.

On-chip voltage conversion [9] is essential for achieving a stable operation of DRAM/SRAM cells with raised supply voltages, and for reducing the subthreshold current with multi V_T and variations in speed, as also discussed before. A high-conversion efficiency, high degree of accuracy in the output voltage, and low power during the standby period are the key issues. The series regulator, which is widely used in modern DRAMs, offers a highly accurate output voltage despite a small output current and a poor conversion efficiency of around 50%.

Testing low-voltage RAMs is problematic. A large subthreshold current makes discriminating defective and non-defective I_{DDQ} currents difficult. Testing the I_{DDQ} by applying a reverse V_{SUB} [37] is effective when low-temperature measurements and multi-V_T designs are combined. The temperature dependence of speed reduced at a lower V_{DD} [38] is another concern.

4. PERSPECTIVES

High S/N designs for RAM cells and arrays, including on-chip ECC circuits to cope with the ever-increasing soft-error rate of RAM cells, and reductions of the subthreshold currents in the active mode are needed to realize low-voltage memories. In the long run, high-speed high-density non-volatile RAMs are attractive for use as low-voltage RAMs. In particular, non-destructive read-out and non-charge-based operations, and the simple planar structures that they could provide, are important to achieving fast cycle and stable operations, even at a lower V_{DD}, at low cost. In this sense, MRAM (magnetic RAM) [39] and OUM (Ovonic Unified Memory) [40] are attractive. For MRAMs, one major challenge is to reduce the magnetic field needed to switch the magnetization of the storage element, while for an OUM, the management of the proximity heating of the cell is an issue. At present, however, the scalabilities and stability reguired to ensure non-volatility still remain unknown, as developments are still in the early stages.

The reduction of subthreshold currents in the active mode may possibly be achieved by using low-power techniques for "old circuits", such as bipolar, BiCMOS, E/D MOS, capacitive boosting, I^2L, and CML circuits. Stand-alone RAMs and e-RAMs, however, could reduce the current by improving the above-mentioned CMOS circuits with the help of new devices, such as the multi-V_T FD SOI. Despite such low-power e-RAMs, however, an SOC will suffer from an incredibly high power dissipated by the random logic gates in the SOC, since control of the subthreshold currents from the random logic gates at a sufficiently high speed may remain impossible. Hence, the number of the gates must be reduced. This presumption implies that new SOC architectures will be required, such as memory-rich SOCs, which effectively reduce the subthreshold currents.

5. CONCLUSION

Low-voltage memory circuits were reviewed with an emphasis on the signal charge of memory cells and subthreshold current reduction. Through the discussion, the need for high-speed non-volatile RAMs, new device/circuits for reducing active-mode subthreshold currents, and memory-rich architectures was discussed.

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