How to Make Efficient Communication, Collaboration, and Optimization from System to Chip

Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology,
2-12-1 Ookayama, Meguro-ku, Tokyo 152-8550, Japan
Tel: +81-3-5734-2508
Email: matsu@ssc.pe.titech.ac.jp

Categories & Subject Descriptors: B.7.0

General Terms: Design

Keywords: SoC, LSI, CMOS, Circuit design, Mixed signal.

1. CURRENT ISSUES OF SOC

SoC (System on a Chip) is a powerful solution to increase system performance and to reduce system cost, in particular for digital consumer products. SoCs for DVD, DTV, DSC, DVC, and cellular phone are current main LSI products for the digital consumer market. However current SoC has tough issues.

1.1 Increase of development time and cost

System complexity has increased along with increase of transistor number. Perfect system verification in a short time is vital. Furthermore physical level verification has become tough, due to the signal integrity and reliability issue.

Mask cost becomes much expensive. Reduction of re-spin is needed. These increase the development time and cost.

1.2 Increase of kind of devices and processes

Current scaled CMOS device and process has tough tradeoffs, not every performance will increase with scaling. The most serious issue is the tradeoff between transistor speed and leakage current. Lower threshold voltage and thinner gate oxide shorten gate delay time, however result in increase of leakage current. SoC for cellular phone needs very low total leakage current of order of mA, however also requires several hundred MHz operation. VT, Tox, Vdd, and Lg should be optimized in transistor. The number of interconnection layers, a set of thickness of metals, a set of wire pitches, and selection of low-k material are also optimized in interconnection. Address for mixed signal technology becomes vital along with highly integration of system in networking and communication era. Analog option should be prepared. MIM or 2PS capacitor, highly accurate resistors with small temperature coefficient, thicker metal for high Q inductor, Varactor, triple well for noise isolation, mediate voltage transistor, such as 1.8V operation, selection of I/O transistor; 3.3V, 2.5V, or 1.8V must be discussed. Embedded DRAM or Flash technology is sometimes needed to increase the competitiveness. These factors and parameters should be optimized for the application of SoC. If failed, The cost and performance doesn't meet the market requirement. This situation tells us that a current advanced SoC will be profitable for only mass market and not suitable for medium and nitch market. Thus the collaboration and optimization from system to device is a key for success in SoC business.

DAC 2003, June 2-6, 2003, Anaheim, California, USA.

2. COLLABORATION AND OPTIMIZATION PROCESS IN SOC DEVELOPMENT

2.1 Making load map

In a long term, making development roadmap is effective collaboration method between every section. Preparing new technologies usually takes long time. The future function, performance, and cost for each application system should be estimated by system peoples, sales peoples, and marketing peoples. Circuit peoples, device peoples, and EDA people should break down the system requirement to each technology and check the possibility and potential tradeoff between required factors. A number of discussions are often needed over the sections to make convergence and increase the validity.

2.2 Optimization of circuit architecture

Development of new circuit architecture often gives sophisticated solution for difficult problems. To find the system bottleneck is the most important work to design SoC. In a SoC for digital TV, the buss occupation is extremely higher than that of conventional CPU for PC and this resulted in low processing speed. Thus parallel bus architecture and cross bar switch technology ware applied and attained two times higher processing speed with same clock frequency [1]. In case of SoC for MPEG4, vector pipeline scheme, dedicated processing unit with hierarchical clock gating was very effective to increase the processing speed with very low power consumption. Designer's insight to system and circuit architecture and the use of hardware emulator to shorten the system verification time is vital for the circuit architecture level design.

2.3 Addressing the mixed signal systems

Modern digital networking, digital communication, digital imaging and digital storage needs mixed signal technology. Thus current SoC for digital consumer products must be addressed to this technology and this requirement increases difficulty for developing SoC in a short time. An average of re-spin in analog LSI is two or three and this number can not be accepted to SoC. This is because mask cost becomes extremely high and time to market is very tight compared to the conventional analog LSI. Thus more powerful and sophisticated design technology is needed [2].

Firstly, perfect system level verification for mixed signal systems is needed before circuit design. Matlab is very good tools to simulate the mixed signal processing in a early system design stages, however C or C++ language often to use for more detail system level design, because of faster simulation time. Mixed mode simulation with Verilog AMS and SPICE should be used in next design stage. More accurate system simulation with acceptable simulation time is possible. Noise effect and some effect to the device mismatch should be simulated in this stage. Theoretical noise model and theoretical data signal are often used, however use of actual noise and signal picked from actual device is recommended. After system level simulation is completed, detail circuit should be designed to realize system requirement. Mismatch check, PVT check, and parameter optimization should be done in this stage. After circuit design, system simulation using this simulated performance in each block should be executed. Also LPE and post layout circuit verification is vital for current analog CMOS circuit. The circuit performance of analog CMOS circuit is strongly effected by parasitic. Global circuit optimization with parasitic is strongly needed. To obtain accurate model and parameter extraction over transistor, interconnect, noise, and mismatch with PVT condition is vital key for success for mixed signal design. Not only top down design flow, but also quick bottom up design flow would be an essentially required for mixed signal design and future digital circuit design. Other important technology in mixed signal SoC is a digital calibration. Analog has an essential tradeoff between accuracy and area. The higher accuracy results in larger area, larger power consumption, and lower frequency characteristic. However requirement for performance and cost is often beyond the optimization. Other reality is that no sufficiently accurate models and parameters are used to be provided in a early development stage. Process is not mature. The digital calibration is very effective method to adjust the circuit characteristics when the power is on. Even if circuit was not optimized or has low accuracy, this method makes the circuit to have proper characteristics. Needed digital circuit becomes smaller with technology scaling, furthermore conventional SoC has some embedded micro controller and no additional controller is needed. Thus this method can be applied easily to current mixed signal SoC.

3. FUTURE OF SOC

A large system will continue to need SoC technology with scaled device; however the number of SoC design will decrease with time. Increase of development time and cost, insufficient performance, insufficient size of market for each application will make the choice of SoC difficult. Embedded circuit of which area is not scalable with technology scaling will make a serious issue in SoC. Cost of this circuit will increase with technology scaling [3]. As a result, large analog circuit and some kind of memory will not able to be embedded in future SoC. SiP (System In a Package) looks strong alternative to address this issue. Different devices; such as different technology nodes, different functions, different materials, and some high performance passive devices can be integrated easily in a package. Conventionally some chips do not to be developed, even if the system configuration and specification are changed. This reduces the development time and cost. Of course, SiP technology has some issues, such as decrease of signal transfer speed, insufficient number of connection, poor design tools, testing and known good die, and reliability. However today is too early to judge this technology is hopeless. We need more time to develop and mature the technology.

4. REFERENCES

[1] A. Matsuzawa, “System On a Chip and low Power Technologies for Digital Consumer Electronics,” Cool Chips, Proceedings, pp.149-173, 2000.

[2] A. Matsuzawa, “High Quality Analog CMOS and Mixed Signal LSI Design,” IEEE International Symposium on Quality Electronic Design, pp.97-104, March, 2001.

[3] A. Matsuzawa, “RF-SoC: Expectations and required condition,” IEEE Transaction on Microwave Theory and Techniques, Vol.50, No.1, pp.245-253, Jan. 2002.