# Figure of merit based selection of A/D converters

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## Abstract

*A new method for selecting analog to digital (A/D) converters based on a generic figure of merit is described. First a figure of merit is introduced that includes both specifications and technology data and that has five generic parameters. The values of these generic parameters can be found by means of a fitting procedure using data from published designs. It is shown that the generic parameters have different values for different types of converters. Therefore the trade-off between speed, resolution, power dissipation and technology parameters depends on the type of converter. This trade-off can than be used to select a particular type of converter for a given application area.*

## 1 Introduction

As a result of the trend of putting more and more digital functionality on a single chip, VLSI technology has continued scaling in both feature size and power supply. As a result of this, analog and mixed signal designers have to work in an ever increasingly challenging technological environment. On the other hand, designers of the crucial analog to digital converter in mixed signal design meet more and more stringent specifications on accuracy, bandwidth and power consumption. To overcome some of this difficulties several solutions for topological choices have been proposed, based on simulation or estimation from a model.

However, all these solutions deal with one type of converter assuming that the choice for this type of converter has already been made. Chosing a certain converter usually is based on rules of thumb. A problem with this method is that it does not take into account possible changes in technology or new design ideas. This paper proposes a more quantitative method to the selection of A/D converter types, based on a figure of merit that has five generic parameters. This figure of merit is introduced in the next section. In section three, general power consumption models are analyzed. Section four describes a fitting procedure for the same parameters based on a survey of published designs. Conclusions are drawn in section five.

## 2 The figure of merit as selection mechanism

To compare different solutions for analog to digital conversion, first a figure of merit must be agreed upon. One of the key insights here is that every design is the product of both designer knowledge and technological 'benefits'. This means that any figure of merit that will be proposed should be normalized with respect to technological values such as supply voltage and minimal feature size. What remains is a figure of merit that quantifies how suitable the architectural choices of a designer for a certain application area are. The proposed figure of merit in this paper is given by:

$$FOM = \frac{a_1^{ENOB} F_b^{a_2} V_{dd}^{a_3} L^{a_4}}{P} a_5 \qquad (1)$$

Where $F_b$ is the input bandwidth, $V_{dd}$ is the supply voltage and $L$ is the minimum feature size. The *ENOB* is the number of effective bits at $F_b$ (i.e. $F_s/2$ for non-oversampling converters). The factor $a_5$ is a scaling factor making the figure of merit 1 for the average design, while the unit of $a_5$ will be chosen such that the total expression is dimensionless. Using this *FOM* a design can be said to be suited for a certain area if its *FOM* is 1 or higher. If it is lower than 1 it means that the particular design is less suited for the area it was used in.

## 3 Bottom up power estimation of generic parameters

In this section an estimate for the different generic parameters is derived based on basic bottom up power estimation for both digital and analog circuitry. For a single digital inverter, the power consumption can be expressed as:

$$P_{dig} = V_{dd} I = V_{dd} F_s C_{gs} V_{sw} \propto V_{dd} V_{sw} F_s C_{ox} W L \propto V_{dd}^2 F_s L \qquad (2)$$

Where it is assumed that the $W$ is proportional and $C_{ox}$ is inversily proportional to $L$ (because of shrinking oxide thickness), which is reasonable for digital circuits. The total power depends on the number of equivalent gates. In general this will increase by maximum a factor two per additional bit of resolution.

For analog circuits, most of the power is consumed in the operational transconductance amplifiers (OTA's) which are present in the circuit. The gain-bandwidth product (which determines the settling time) of these OTA's is proportional to the sampling frequency [4].

$$F_s \sim \frac{gm}{2\pi C_{tot}} = \frac{2I}{2\pi (V_{gsT}) C_{tot}} \tag{3}$$

If the accuracy of the circuits is limited by thermal noise, the size of the capacitor needs to be [3]

$$C_{tot} = \frac{4kT(DR)}{V_{sw}^2} \tag{4}$$

Where $V_{sw}$ is the maximum signal swing and *DR* is the dynamic range of the system. This lead to the following expression for the power consumption of the analog circuitry.

$$P = V_{dd} I \propto \frac{V_{dd} F_s V_{gsT} 4kT DR}{V_{sw}^2} \tag{5}$$

This equation shows that for an increase of one bit in accuracy (i.e. 6.02 dB in dynamic range) about a factor four more power is consumed. An increase in bandwidth of a factor two means an proportional increase in power consumption. Assuming $V_{gsT}$ and $V_{sw}$ do not scale proportionally to the supply voltage, the dependence on the this supply voltage will be about 1. The dependence on the minimum feature size will in general be small. Above derivation was performed assuming thermal noise and settling time of the OTA's where the major bottlenecks. Similar derivations can be made when the expected bottlenecks are capacitor or offset mismatch or when the slew-rate of the OTA's is important. All these derivations lead to similar expressions for the power (except for dependence on supply voltage and minimum feature size), which has come to known as the speed-power-accuracy trade-off [1]. The actual trade-off in a complex system such as an A/D converter depends on the amount of analog versus digital power and whether techniques such as digital calibration, averaging or dynamic element matching are used.

## 4 Fitting of the generic parameters

To be able to esimate the paramters of the *FOM* a fitting procedure is be used similar to [2]. The parameters will be fitted using data from actual implementation of three types of converters flash, pipeline and (the analog portion of) Delta Sigma modulators, published in recent years in both the IEEE Journal of Solid State Circuits and the proceedings of the International Solid-State Circuits Conference. For the Delta-Sigma modulator only the low-pass kind is considered. The fitting process is performed using a least mean squares error (LMS) criterion. Using this criterion it is possible to estimate the model correctness using the chi-square test. The results of the fitting procedure for the different converter types are listed in table 1. The probability of the correctness of the model was 80% for flash converters and Delta-Sigma modulators and 50% for pipeline converters. The value of $a_1$ is always much smaller than four.

**Table 1. Fitted values for the parameters $a_{1-5}$, $\sigma$ expresses the standard deviation.**

| type | $a_1$ | $a_2$ | $a_3$ | $a_4$ | $a_5$ | $\sigma$ |
|---|---|---|---|---|---|---|
| flash | 1.6 | 1.05 | 1.18 | 1.23 | 0.0683 | 1.31 |
| pipel. | 1.24 | 0.79 | 2 | 0.04 | 0.241 | 1.71 |
| $\Delta\Sigma$ | 1.78 | 0.76 | 1.4 | 0.18 | 0.006 | 2.18 |

This shows that for all structures, the speed-power-accuracy trade-off was not governing the performance. This is probably due to fact that analog performance can be improved by the use of digital circuitry (such as is the case with digital calibration). The value of $a_3$ shows that for pipeline probably the digital circuitry consumes most power. For the other structures the consumption is divided more or less equally between analog and digital components. Furthermore, $a_4$ shows that only for the flash converter there is a real benefit of the smaller feature size. The estimated parameters make it possible to choose between different converter types by calculating the estimated power consumption based on the technology and the target specifications.

## 5 Conclusions

A selection strategy for analog to digital converters based on a generic figure of merit was presented. The generic parameters where estimated using a fitting procedure on published designs and it was shown that different converer architectures exhibit different trade-offs.

## References


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