A Slew Rate Enhancement Technique for Operational Amplifiers based on a Tunable Active G_m-based Capacitance Multiplication Circuit

Ram Suryanarayan
Dept. of Electrical Engineering
University of Virginia
Charlottesville, VA 22904
434-982-2965
rsn2g@virginia.edu

Anubhav Gupta
Dept. of Electrical Engineering
University of Virginia
Charlottesville, VA 22904
434-982-2965
anubhav@virginia.edu

Travis N. Blalock
Dept. of Electrical Engineering
University of Virginia
Charlottesville, VA 22904
434-924-1331
blalock@virginia.edu

ABSTRACT

A slew rate enhancement technique for operational amplifiers using a tunable active G_m-based current-mode capacitance multiplication circuit instead of the standard Miller compensation capacitor is developed. Low power and low area solutions for driving large capacitive loads are enabled by this technique. In a prototype amplifier, a 0.5 pF MOSFET is multiplied to an effective value of 285 pF, setting the dominant pole at 3 Hz. The slew rate, however, is controlled by the physical MOSFET capacitor. A slew rate as high as 1.5 V/μs is obtained for a standard two stage folded cascode opamp with a 2.5 μA differential pair tail current. An open loop gain of 101 dB and a phase margin of 56° are observed.

Categories and Subject Descriptors

B.7.1 **[Integrated Circuits]**: Types and Design Styles – *advanced technologies*.

General Terms

Design.

Keywords

CMOS, opamp, operational amplifier, slew rate, compensation, feedback.

1. INTRODUCTION

An operational amplifier must operate with stability with different types of passive feedback, varying loads, temperatures and processes. To enable this, the operational amplifier must behave like a one pole system all the way up to its unity gain frequency. Hence, the first pole should be orders of magnitude lower than the others, in order that the open loop gain is not compromised. In order to have the first pole at a very low frequency, we need large compensation capacitors. Miller compensation has traditionally been used to take advantage of the high gain of the output stage [1]. However, Miller compensation leads to a zero, which reduces the phase margin. In order to get over this problem, cascoded Miller compensation and cascoded nested Miller compensation schemes have been used, which introduce additional poles and also additional power. Hence, the standard, simple Miller compensation is more suitable for very low power applications [2]. The simple Miller compensation is also less sensitive to parameter variations than the cascoded and nested cascoded forms [2]. Nevertheless, there is the problem of the feedforward zero. Our approach avoids the feedforward path, at the same time extracting the $g_m r_o$ gain of a transistor. The dominant pole is taken to a very low frequency, making the amplifier robust to parameter and load variations. The slew rate is controlled by a small physical capacitor, C_p.

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Fig.1 shows the basic concept of the current-mode capacitor multiplication technique. A small physical capacitor, C_p, is placed in series with a current sensing circuit. The sensed small signal current is then multiplied by a gain factor, K, and fed back into the circuit input terminal. The operation results in the driving circuit being loaded by an equivalent capacitance equal to $C_p(K+1)$. This approach is presented in [3], in an excellent application of this concept to the frequency compensation of a linear regulator. Our circuit is different in implementation and offers lower equivalent series resistance, larger multiplication factors, and is tunable.

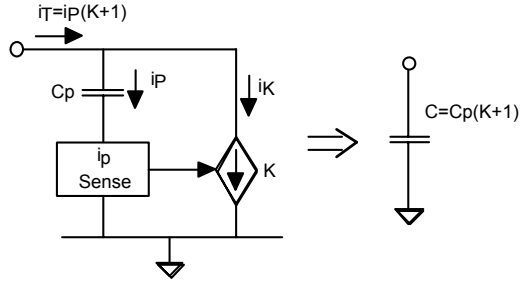

Figure 1. Current-mode capacitance multiplication concept.

The primary limitations of the current-mode capacitor multiplication approach are bandwidth and quality factor, which is due to equivalent series resistance (ESR) and parallel resistive loading. Bandwidth is limited by the speed of the sensing and

current multiplication circuits. ESR is limited by the impedance of the current sensing circuit and parallel loading is constrained by the output impedance of the current generation circuit. Other limitations of the approach include constraints on the voltage swing, which depend upon the biasing needs of the current sensing circuit and the capacitor bias voltage, which may be particular to a process technology.

2. G_M-BASED CURRENT-MODE CAPACITANCE MULTIPLICATION

Fig.2 is a simplistic schematic of our Gm-based capacitance multiplication circuit. C_p is the physical capacitance of 0.5 pF in our prototype circuit. Devices M5, M6, and M9 form a negative feedback circuit which create a virtual ground at the bottom plate of C_p. The virtual ground impedance, R_x, is approximately given by

$$R_X = \frac{1}{g_{m6}(A_{GDM9}A_{GSM6})} \qquad (1)$$

i.e., the impedance looking into M6 divided by the loop gain [4]. The ESR for the complete circuit is $R_x/(1+K)$. The circuitry on the right of M2 is identical to that on the left of M1 except for the physical capacitor C_p and the input connection. V_{b1} is the bias generated by the circuitry on the right. The 10 µW prototype circuit has an active capacitance with an ESR of 10 ohms. This can be reduced with increased power.

Assuming the impedance looking into M6 is much lower than r_{o5}, the small-signal capacitor current, i_P, flows through M6 and gives rise to a small-signal voltage $i_P r_{o7}$ at the gate of M1 (the output impedance of M6 is high due to the large impedance seen looking out of the source).

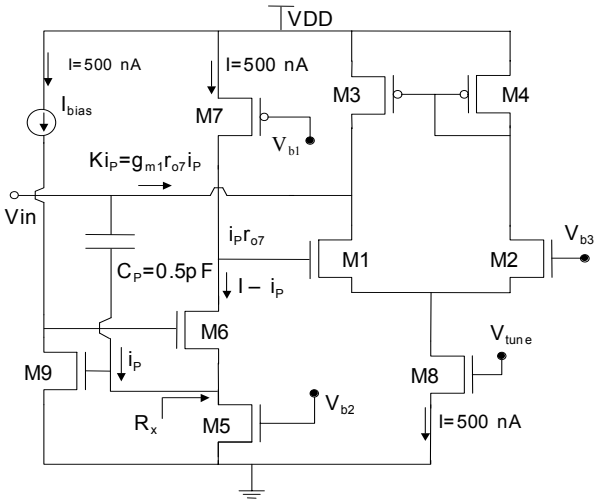

Figure 2: Gm-based current-mode capacitance multiplier circuit schematic.

Given the $i_P r_{o7}$ excitation at the gate of M1, the current-mirror differential pair produces an output current of $g_{m1}r_{o7}i_P$. The total current seen at Vin is $i_P(1+K)$, where $K = g_{m1}r_{o7}$, corresponding to a total capacitance of $C_p(1+K)$ at Vin. Tuning of the capacitance is accomplished by varying V_{tune}. The tuning capability adds design flexibility as compared to a standard Miller capacitor. We will refer to the current through M8 as the tuning current of the active capacitor.

In order to improve the quality factor, Q, of the capacitor, the output of the differential pair is cascoded. This increases output resistance, thereby reducing Vin/ro currents, which would otherwise give rise to a loss term and reduce the quality factor. The current source M7 is cascoded in order to increase the output resistance as seen from the gate of the differential pair. This results in a higher small signal voltage at the gate of M1 and hence higher multiplicative gain factor K. A schematic of the active capacitor with the cascoded structures is shown in Fig.3.

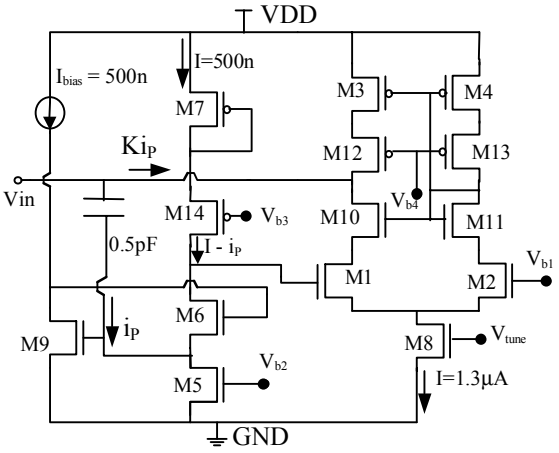

Figure 3. Cascoded version of the g_m-based capacitor multiplier .

3. PROTOTYPE OPERATIONAL AMPLIFIER

The opamp used has a standard two stage folded cascoded topology. Fig. 4 is a schematic of the opamp. The active capacitor input terminal is connected to node X in the figure. The rectangular box shown is the active capacitor of Fig. 3. Thus, we have an effective capacitance of $(K+1)C_p$ at node X. The opamp has not been optimised for input and output voltage swings. The second stage is a class A output stage.

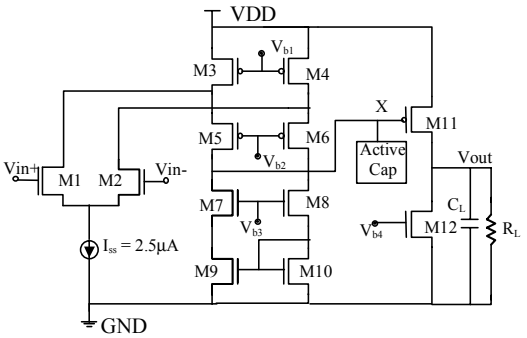

Figure 4. Folded cascode opamp with active capacitor compensation.

The emphasis is to show a slew rate enhancement technique and also a low area, low power solution for compensation, eliminating the feedforward path. The large signal speed of opamps in general

may be limited by the slew rate simply because the current available to charge and discharge the dominant capacitor is small [5]. When the circuit enters a slewing condition, the active capacitor in Fig. 4 would need $(1+K)I_{ss}$ to charge node X, which cannot flow into the capacitor if the tuning current of the active capacitor is lower than $(1+K)I_{ss}$. If this condition holds, slew rate enhancement is observed. This current starvation gives rise to a higher slew rate but does result in a small penalty on settling time during slew recovery for fast rising steps.

4. SIMULATION RESULTS

The g_m-capacitor circuit of Fig. 3 is biased at 1.3 µA. The output impedance of the active capacitor is as high as 400 MΩ. The simulated current and voltage phase responses of the active capacitor are shown in Fig. 5. The phase difference stays close to 90° for almost five decades. We can say that the bandwidth of the capacitor is five decades. Fig. 6 shows the capacitor multiplication factor (i_K/i_P) plotted against frequency. The ratio is seen to be constant at around 570 for frequencies between 5 Hz and 100 KHz (close to five decades). This means that the 0.5 pF physical capacitor is converted into a 285 pF effective capacitance, which reduces the on-chip capacitor area by a factor of 570. This moves the dominant pole of the cascoded opamp to 3 Hz. The opamp drives a 20 pF, 100 KΩ load. An open loop gain of 101 dB with a phase margin of 56° is obtained. The high open loop gain can be attributed to high output resistances due to low current and cascoded structures. The open loop magnitude and phase responses are shown in Fig. 7. The differential pair tail current is 2.5 µA. Since the active capacitor tuning current is 1.3 µA, i.e., lower than KI_{ss} , the slew rate enhancement condition holds. The time domain large signal settling response for a 1V step at the input is shown in Fig. 8. The rise time of the step input is 2ns.

The slew rate corresponding to the multiplied capacitance is $I_{ss}/C_{effective}$ = 2.5 µA/285 pF = 0.00877 V/µs, while the slew rate corresponding to the small physical capacitance is I_{ss}/C_p = 2.5 µA/0.5 pF = 5 V/µs. The slew rate obtained in simulation is 1.5 V/µs.

Thus, the slew rate obtained in simulation is much higher than the case with a 285 pF physical capacitor at node X. The slew rate is close to that corresponding to the smaller physical capacitor. This value of slew rate is lower than that corresponding to the smaller capacitor because of parasitic capacitances inside the active capacitor and the ESR. The time domain slewing response shows an undesired dip before settling to the final value, as seen in Fig. 8. This is because the input node X can charge up C_p faster than the rest of the active circuitry, which normally absorbs K times the current through C_p. In the slewing condition, the active circuitry is temporarily current starved, but after a short delay begins to generate the multiplicative current causing a drop in the voltage as the driving circuit begins to respond to the current increase. The voltage drop is lower if the step input has a smaller slope (longer rise time). Improvement of the amplifier's recovery from the slewing condition is the subject of future analysis and simulation.

A non-cascoded version of the opamp has also been simulated with the active capacitor of Fig. 2. This opamp drives on-chip capacitive loads (C_L = 100 fF). A comparison between the simulated the cascoded and non-cascoded version is shown in Table1.

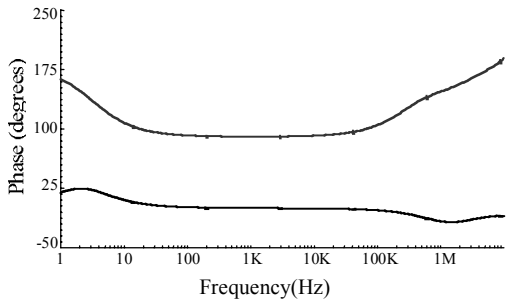

Figure 5. Current and voltage phase plots for the active capacitor.

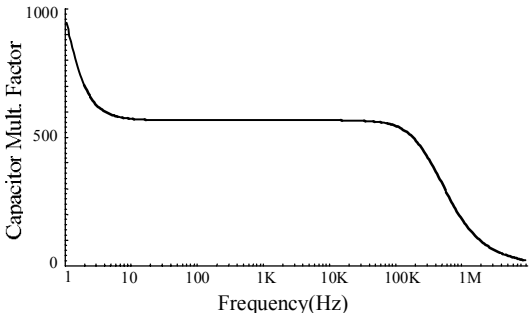

Figure 6. Active capacitor multiplication factor vs frequency.

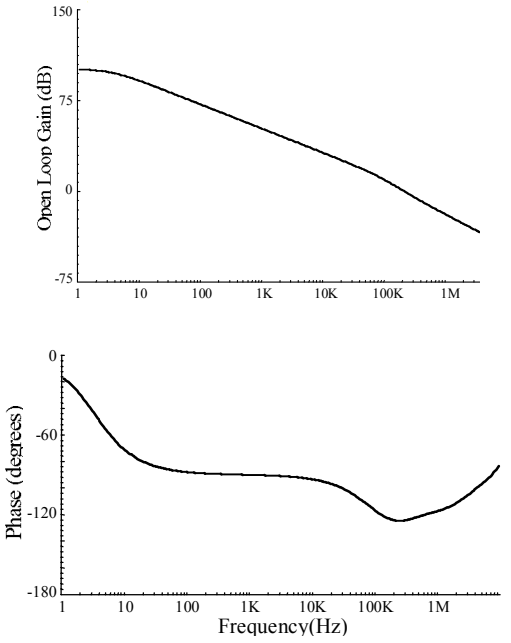

Figure 7. Open loop gain and phase responses of the amplifier.

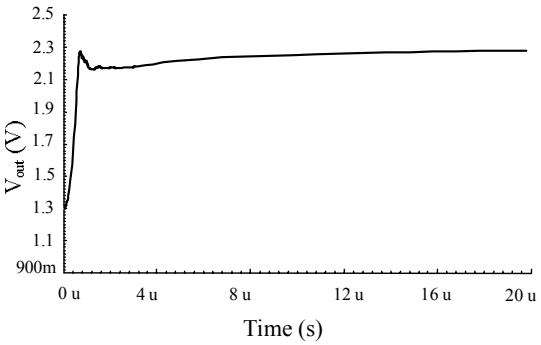

Figure 8. Large signal settling of cascoded opamp for a 1V step input. R_L = 100 K and C_L= 20 pF (off-chip load).The slew rate is 1.5 V/µs.

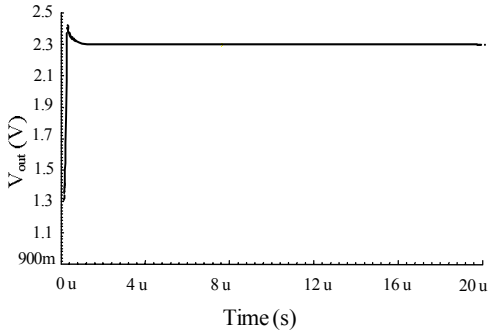

Figure 9. Large signal settling of the non-cascoded opamp for a 1V step input with C_L = 100 fF (on-chip load). The slew rate is 6.6 V/µs.

Table 1. Comparison between simulated results of the cascoded and non-cascoded opamps

	Cascoded	Non-Cascoded
Opamp tail current (µA)	2.5	0.9
Active capacitor tuning current	1.3	0.5
Slew rate (V/µs)	1.5	6.6
Open loop Gain (dB)	101	77
Open loop Band-width (KHz)	210	3700
Phase Margin (degrees)	56	69
Opamp Area (μ^2)	120	30
Power (µW)	133	11
Capacitance mul-tiplication factor	570	175

5. EXPERIMENTAL RESULTS AND CONCLUSIONS

A simple two stage opamp (non-cascoded version) with the active capacitor of Fig. 2 has been built and tested in a 0.25 micron TSMC CMOS process. Early experimental results show the slew rate is 6.9 V/µs for a 1V step at the input, which comes close to the simulated value of 6.6 V/µs. The differential pair bias current of the opamp is 900 nA. The slew rate corresponding to the small physical MOSFET capacitor (0.1 pF in this case) is given by I_{ss}/C_p = 9 V/µs. This value is close to the value of slew rate obtained experimentally. The multiplication factor is found to be 170. The multiplication factor is determined by characterizing a test structure of the active capacitor. We observe a slew rate corresponding to the smaller 0.1 pF capacitor and the compensation effects of a larger 17 pF capacitor.

A low area, low power slew rate enhancement technique for opamps has been developed. The two-stage opamp achieves a high gain bandwidth product with a good phase margin. It shows a high slew rate for small bias currents. Since the bandwidth of the capacitor is restricted to a few hundred KHz, the capacitor and the opamp are both suitable for low frequency applications. The G_m-based capacitance multiplication technique reduces on chip capacitor area by two to three orders of magnitude when substituted for a standard MOSFET capacitor in low frequency applications. Further work will be directed towards increasing the bandwidth of the active capacitor and improving the recovery from slew rate limited transients.

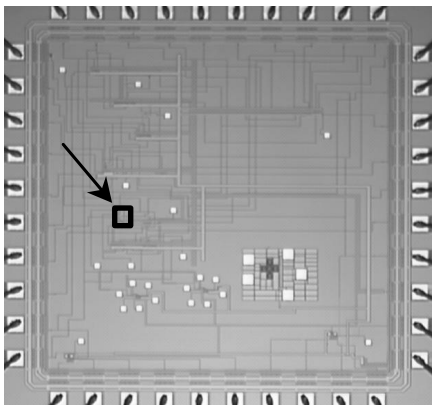

Figure 10. Photomicrograph of the test chip.

6. REFERENCES

[1] R. G. H. Eschauzier and J. H. Huijsing, "Frequency Compensation Techniques for Low-Power Operational Amplifiers," Kluwer Academic Publishers, Dordrecht, Netherlands, 1995.

[2] R. Hogervorst and J. H. Huijsing "Design of Low-Power Operational Amplifier Cells," Kluwer Academic Publishers, 1996.

[3] G. A. Rincon-Mora, "Active Capacitor Multiplier in Miller-Compensated Circuits," IEEE J. Solid State Circuits, vol. 35, no. 1, pp. 26-32, Jan. 2000.

[4] K. Bult and G. Geelen, "A fast settling CMOS op-amp for SC circuits with 90 dB DC gain," IEEE J. Solid State Circuits, vol. 25, no. 12, pp. 211-213, Dec. 1990.

[5] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2000.