Modeling of Ballistic Carbon Nanotube Field Effect Transistors for Efficient Circuit Simulation

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ABSTRACT

Carbon Nanotube Field-Effect Transistors (CNFETs) are being extensively studied as possible successors to CMOS. Novel device structures have been fabricated and device simulators have been developed to estimate their performance in a sub 10nm transistor era. This paper presents a novel method of circuit-compatible modeling of CNFETs in their ultimate performance limit. The model so developed has been used to simulate arithmetic and logic blocks using HSPICE.

1. INTRODUCTION

Aggressive scaling of CMOS circuits has led to higher and higher integration density, more functional complexity and better performance. However, with "short channel effects" in the way of scaling these nano transistors, research has started in the earnest to look for possible alternatives. Carbon nanotube transistors have emerged as possible alternatives to silicon transistors.

The theory of carbon nanotube transistors is still primitive and the technology is still nascent [1-3]. However, evaluation of such high performance transistors in digital circuits is absolutely essential to drive the device design and understand the bottlenecks in multi-Gigahertz processor design. But from a circuit designer's point of view, circuit simulation and evaluation using CNFETs is challenging because most of the developed models are numerical, involving self-consistent equations which circuit solvers like SPICE are not able to handle. This paper presents a novel surface potential based SPICE compatible modeling technique for carbon nanotubes in their ballistic limit of performance with 1-D electrostatics This model uses suitable approximations necessary for developing any quasi-analytical, circuit-compatible compact model. Both I-V and C-V characteristics have been modeled. This simple model enables simulation of circuit transfer (dc) characteristics as well as transients. It has been validated against numerical models in [4, 9] and has been found to be in very close agreement. It has been incorporated in SPICE and has been used to simulate digital logic blocks, functional and processing units.

The novelty of the paper lies in the fact that for the first time a simplistic model has been developed to assess circuit performance of CNFETs. It enables us to evaluate delays, estimate power in logic circuits and simulate the performance degradation due to interconnect and device parasitics. Also, this modeling technique is generic in the sense that it can faithfully represent a wide range of CNFET geometries and gate materials with reasonable operating voltages and user specified temperature conditions. The beauty of such a model is in its strong foundation on the underlying physics of operation along with necessary simplifications and assumptions. This makes a multiple-transistor circuit simulation possible.

2. BALLISTIC CNFETs

2.1 Ballistic CNFETs

Current research has identified two possible CNFETs based on their modes of operation. The first one is a ballistic CNFET where the channel is intrinsic and has doped source/ drain regions. The second type has metallic source/ drain regions and the transport through the channel is governed by the tunneling of electrons through a Schottky barrier at the source and channel junction. These two types of nanotubes have been shown in Fig 1. In this paper we will consider the first type of nanotubes since they provide higher on-current and near ideal subthreshold slope. Thus these transistors would define the upper limit of performance.

2.1 Theory of Ballistic CNFETs

The computational procedure for CNFETs is given below [1]:

A) Consider a particular value of V_{DS}, and beginning-of-channel control potential ψ_S . The control voltage, is the amount by which the energy bands move up or down due to the application of a gate voltage V_G.

B) Compute the total charge on the nanotube for a given V_{DS} and ψ_S. The charge at the top of the barrier has contributions from both the source and the drain. All the +k states at the barrier-top are filled by the source while the –k states are populated by the drain [1]. Thus

$$n_{CNT} = \int_{E_C}^{+\infty} \frac{D(E)}{2} \left[f(E-\mu_S) + f(E-\mu_D) \right] \cdot dE \qquad (1)$$

where n_{CNT} is the number of carriers in the channel, μ_S (μ_D) is the source (drain) Fermi level, E_C is the bottom of the conduction band, f(E) is the probability that a state with energy E is occupied (Fermi-Dirac distribution) and $D(E)$ is the nanotube density-of-states (DOS). Thus the total charge for each sub-band can be thought of as the sum of the charges contributed by the source and the

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drain, individually. Also let us assume the source Fermi level as the reference level and hence, $\mu_s = 0$ and $\mu_D = -qV_{DS}$ where q is the electronic charge.

C) Drain current I_D for each sub-band is obtained as:

$$I_D = \frac{4ek_BT}{h}\left[\ln(1+\exp(-\xi_S)) - \ln(1+\exp(-\xi_D))\right] \quad (2)$$

$$\text{where } \xi = \left(\frac{\Psi_S - \Delta_1 - \mu}{KT}\right) \quad (3)$$

D) The gate bias V_G required to produce the assumed ψ_S based on the electrostatic capacitance relations of the capacitance model is determined as:

$$\psi_S = V_G - \frac{Q_{CNT}}{C_{INS}} \quad (4)$$

where C_{INS} is the insulator capacitance.

E) Finally, we obtain the gate potential applied V_G' to

$$V_G' = V_G + V_{FB} \quad (5)$$

determine the effective gate bias V_G from where V_{FB} is the flat-band voltage. In the rest of the paper V_G will be referred to as V_{GS} because all potentials will be measured with respect to the source potential.

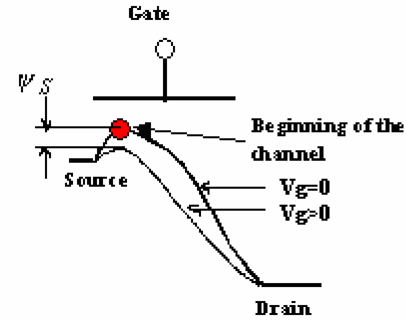
By repeating step A) to E) for a set of (ψ_S, V_{DS}) points, the $I_D(V_{GS}, V_{DS})$ characteristics can be obtained. A Matlab® script that performs this calculation is available in [2].

3. A SPICE COMPATIBLE COMPACT MODEL FOR THE CNFET

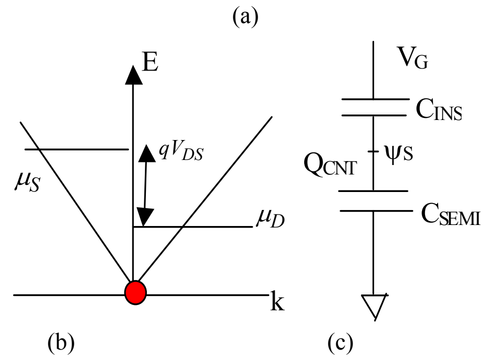
It has already been discussed that modeling the CNFET requires solving the self consistent potential ψ_S. The presence of the self-consistent loop in the flow makes SPICE simulations impossible. So a SPICE compatible model for CNFETs is required. The next three sections explain the development of such a model.

3.1 Quantum charge computation

The charge at the beginning of the channel is given by (9)–(14). It is not possible to obtain an analytical closed form expression for the integral given in (14) and curve fitting has been resorted to. It can be noted that the number of carriers, n increases almost linearly as ξ becomes more and more positive and it falls off exponentially as ξ becomes negative. Hence a reasonably good fit will be.



(a)



(b) (c)

Figure 1 (a) The subband profile vs. the channel position at a high drain bias and. (b) The +k states at the beginning of the channel are filled by the source Fermi level and the –k by the drain Fermi level. The control voltage ψ_S moves the E-K diagram rigidly up and down. (c) The capacitor equivalent network. C_{SEMI} is the semiconductor capacitance.

$$n / N_0 = A\exp(\xi) \quad \text{for } \xi < 0 \quad (6a)$$

$$= B\xi + C \quad \text{for } \xi \geq 0 \quad (6b)$$

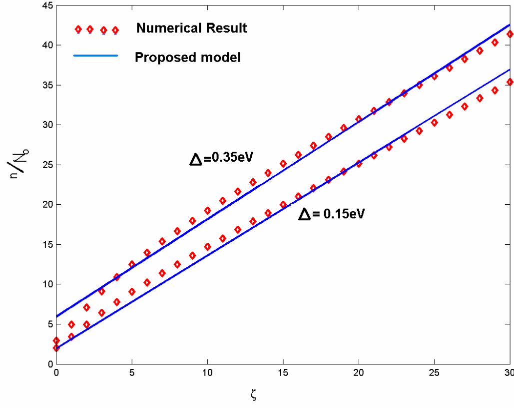
To maintain continuity at ξ=0 we require A = C. It should be noted that the parameters A and B are functions of Δ. For an operating voltage (Vdd) of 500mV, all conduction bands below 500mV are of concern. For Δ<0.5eV, A and B can be expressed empirically as polynomials of Δ (in eV) as,

$$A = -5.3\Delta^2 + 10\Delta + 1 \quad (7)$$

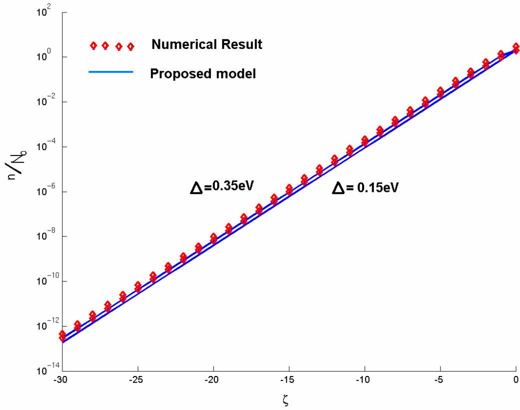
$$B = 0.34\Delta + 1 \quad (8)$$

3.2 Determination of the surface potential

The next step in the model development is to relate the control potential ψ_S with the effective gate bias V_{GS}. It can be noted that when the gate bias V_{GS} is less than the first equilibrium
conduction band minima, Δ_1, the total charge across the C_{ins} is very low and the control potential ψ_S follows the gate voltage V_{GS} (vide equation 4). Once the gate voltage exceeds Δ_1 there is considerable charge buildup across



(a)



(b)

Figure 2: (a) Plot of n/N$_0$ vs. ζ for positive values of ζ for two different values of Δ. (b) Plot of n/N$_0$ vs. ζ for negative values of ζ for two different values of Δ.

C_{ins} and the surface potential can no longer follow the gate voltage V_{GS}.

The voltage drop across C_{ins} is approximately linear with V_{GS} as long as the latter does not exceed 700mV. This is intuitive because the charge built up for ξ>0 has been noted to be an approximate linear function of ξ. Thus ψ_S and V_{GS} can be approximately related by the following simple equations.

$$V_{GS} - \psi_S = 0 \quad \text{for } V_{GS} < \Delta_1 \tag{9a}$$

$$= \alpha(V_{GS} - \Delta_1) \quad \text{for } V_{GS} \geq \Delta_1 \tag{9b}$$

where Δ_1 is the equilibrium sub-band minima of the first sub-band. However the slope of the curve, α is a function of the applied V_{DS} and the device parameters. α can be expressed as a polynomial of V_{DS} as shown below:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \tag{10}$$

For a device of diameter 3nm and 17pF/m of insulator capacitance, $\alpha_0 = 0.31$, $\alpha_1 = -0.36(Volts^{-1})$ and $\alpha_2 = 0.10\,(Volts^{-2})$. For another device of diameter 5nm and 30pF/m of insulator capacitance, $\alpha_0 = 0.19$, $\alpha_1 = -1.10(Volts^{-1})$ and $\alpha_2 = 1.40(Volts^{-2})$.

Thus the control potential can be related to the gate bias as,

$$\psi_S = V_{GS} \quad \text{for } V_{GS} < \Delta_1 \tag{11a}$$

$$= V_{GS} + \alpha(V_{GS} - \Delta_1) \text{ for } V_{GS} \geq \Delta_1 \tag{11b}$$

Once ψ_S is known as a function of V_{GS}, the drain to source current, I_{DS} can be easily computed from (2).

3.3 Quantum capacitance computation

With the knowledge of charge and surface potential as functions of gate bias, the gate input capacitance C_G can be computed in terms of the device parameters and the terminal voltages. The gate-input capacitance is given by:

$$C_G = \frac{\partial Q_{CNT}}{\partial V_{GS}} \tag{12}$$

$$\Rightarrow C_G = \frac{\partial Q_{CNT}}{\partial \psi_S} \cdot \frac{\partial \psi_S}{\partial V_{GS}} \tag{13}$$

The total charge Q_{CNT} can be split up into Q_S and Q_D, the separate contributions from the source and the drain, and hence, the total gate capacitance can also be split up into C_{GS} and C_{GD}.

Depending on the region of operation we have, the expressions for capacitance given in Eqn. 14

$$C_{Gi} = qN_0 \frac{AL}{KT} \exp(\xi_i) \quad \text{for } \xi_i < 0 \;\&\; V_{GS} \leq E_{C1} \tag{14a}$$

$$= qN_0 \frac{AL}{KT} \exp(\xi_i)(1-\alpha) \quad \text{for } \xi_i < 0 \;\&\; V_{GS} \geq E_{C1} \tag{14b}$$

$$= qN_0 \frac{BL}{KT} \quad \text{for } \xi_i \geq 0 \;\&\; V_{GS} \leq E_{C1} \tag{14c}$$

$$= qN_0 \frac{BL}{KT}(1-\alpha) \quad \text{for } \xi_i \geq 0 \;\&\; V_{GS} \geq E_{C1} \tag{14d}$$

for i=s,d and L is the nanotube length

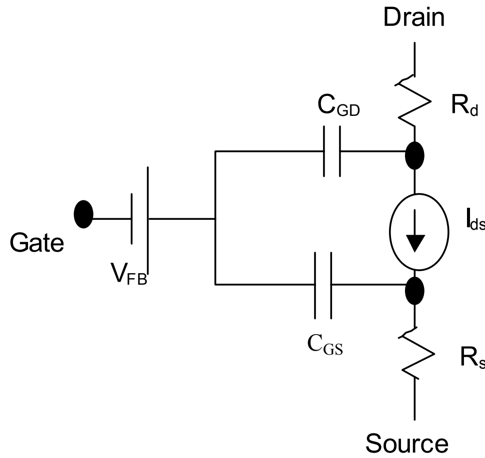


Figure 3: Spice compatible circuit model of the ballistic one-dimensional CNFET

As in case of charge computation, the total capacitance has to be computed for each filled conduction sub-band and they should be added in parallel.

An important aspect of modeling is the extraction of the fitting parameters from an experimental device. In the model developed, the parameters A and B depend on the nanotube radius and can be easily determined. The fitting parameters α_0, α_1 and α_2 can be extracted from the I_{DS}-V_{GS} characteristics of the device. Three data-points would be required to solve a set of three nonlinear equations and the fitting parameters can be obtained.

4. VERIFICATION OF THE MODEL

Fig. 3 shows the schematic diagram of the proposed model. Fig. 4 shows how the proposed model corroborates with the numerical data. It has been used to simulate dc as well as transient circuit characteristics. Fig. 5 shows the voltage transfer characteristics of a CMOS logic inverter with two different values of the flatband voltage.

5. CONCLUSION

A novel technique for CNFET modeling for circuit applicaitions has been developed. This has been used to perform dc and transient simulations.

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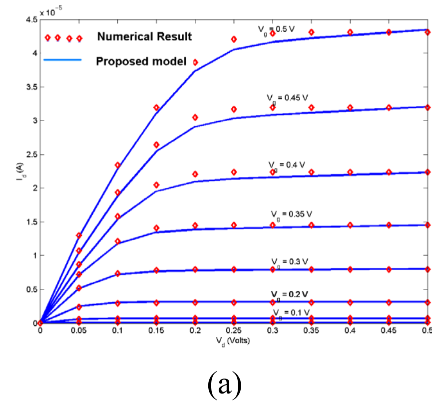
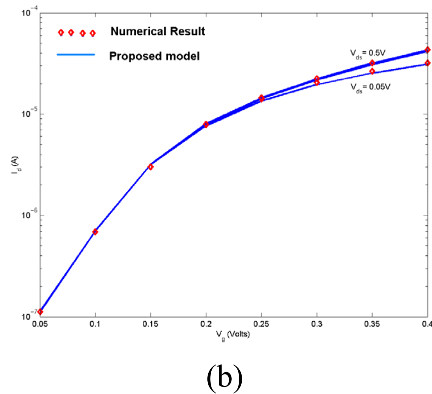


(a)



(b)

Figure 4: (a) Plot of I_D vs. V_{DS} for different values of V_{GS}. (b) Plot I_D vs. V_G for different values of V_{DS} for a CNFET of diameter (d) = 3nm and C_{ins} = 17pF/m

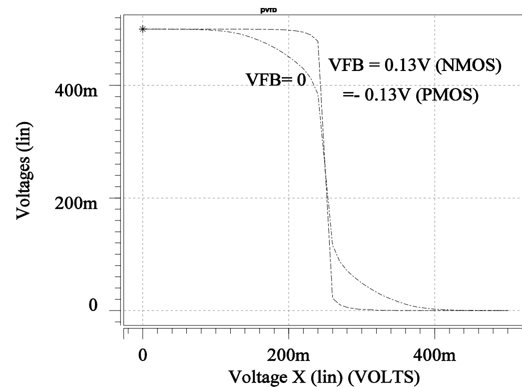


Figure 5: VTC of an inverter for two different values of V_{FB} (NFET=0 PFET=0); (NFET=0.13 PFET=-0.13)