Energy Recovery Clocking Scheme and Flip-Flops for Ultra Low-Energy Applications

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ABSTRACT

A significant fraction of the total power in highly synchronous systems is dissipated over clock networks. Hence, low-power clocking schemes would be promising approaches for future designs. We propose four novel energy recovery flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. Based on the simulation results using TSMC 0.25μm CMOS process technology, at a frequency of 200MHz, the proposed flip-flops exhibit more than 80% delay reduction, power reduction of up to 46%, and area reduction of up to 77%, as compared to the conventional energy recovery flip-flop. We implemented 1024 proposed energy recovery flip-flops through an H-tree clock network driven by a resonant clock-generator that generates a sinusoidal clock. Results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using the conventional square-wave clocking scheme and flip-flops.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, microprocessors and microcomputers, VLSI.*

General Terms: Theory and Design

Keywords: Adiabatic, Clock, Clock Tree, Energy Recovery, Flip-Flop

1. INTRODUCTION

Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. The increasing demand for high-performance VLSI System-on-Chip (SOC) designs is addressed by increasing the clock frequency and integrating more components on a chip, enabled by the continuing scaling of the process technology. With the continuing increase in the clock frequency and complexity of high-performance VLSI chips, the resulting increase in power consumption has become the major obstacle to the realization of high-performance designs. In addition to increased cooling costs, increased power consumption shortens the battery lifetime in portable applications. The major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. In the Itanium[TM]

microprocessor, more than 30% of the total chip power is due to the clock distribution network [1]. Thus, innovative clocking techniques for decreasing the power consumption of the clock networks are required for future designs.

Energy recovery is a technique originally developed for low-power digital circuits [2]. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an AC-type (oscillating) supply voltage [2]. In this paper, we apply energy recovery techniques to the clock network since the clock signal is typically the most capacitive signal. The proposed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal. The rest of the system is implemented using standard circuit styles with a constant supply voltage. However, for this technique to work effectively, there is a need for energy recovery flip-flops that can operate with a sinusoidal clock. A pass-gate energy recovery flip-flop has been proposed in [3] that works with a four-phase sinusoidal clock. The main disadvantage of the pass-gate energy recovery flip-flop is that its delay takes a major fraction of the total cycle time; therefore, the time allowed for combinational logic evaluation is significantly reduced. In addition, it requires four phases of the clock, adding considerable overhead to clock generation and routing.

In this paper, we propose four high-performance and low-power energy recovery flip-flops that operate with a single-phase sinusoidal clock. The proposed flip-flops exhibit significant reduction in delay, power, and area as compared to the conventional four-phase pass-gate energy recovery flip-flop. We integrated 1024 energy recovery flip-flops distributed across an area of 4mm × 4mm and clocked through an H-tree clocking network. A resonant clock-generator circuit was designed to generate a sinusoidal clock and drive the clock network and the flip-flops. For comparison, we implemented the same clock-tree using square-wave clocked flip-flops. In this case, the clock network is buffered by a chain of progressively sized inverters.

The remainder of this paper is organized as follows. In section 2, the conventional four-phase pass-gate energy recovery flip-flop is reviewed and the proposed energy recovery flip-flops are described. In section 3, extensive simulation results of individual flip-flops and their comparisons are presented. Section 4 includes system integration, clock generation and the clock-tree implementation. Finally, the conclusion of the paper appears in Section 5.

2. ENERGY RECOVERY FLIP-FLOPS

In this section, our proposed flip-flops, as well as the conventional energy recovery flip-flop, are presented and their operations are discussed. Figure 1 shows the schematic of a conventional Four-Phase Transmission-Gate (FPTG) energy

recovery flip-flop [3]. FPTG is similar to the conventional Transmission-Gate Flip-Flop (TGFF) [4] except that it uses 4-transisor pass-gates designed to conduct during a short fraction of the clock period. The energy recovery clock is a four-phase sinusoidal clock (CLK0, CLK1, CLK2, and CLK3) as shown in Figure 2. FPTG is a master-slave flip-flop with the master controlled by CLK0 and CLK2 and the slave controlled by CLK1 and CLK3. The main disadvantage of this flip-flop is its long delay. As shown in Figure 2, the delay from D to Q (t_{D-Q}) takes roughly half the effective clock period (T_{eff}). In addition, transistors required for the pass-gates are large, resulting in large flip-flop area.

Another approach for energy recovery flip-flops is to locally generate square-wave clocks from a sinusoidal clock [3]. This technique has the advantage that existing square-wave flip-flops could be used with the energy recovery clock. However, extra energy is required in order to generate and possibly buffer the local square waves. Moreover, energy is not recovered from gate capacitances associated with clock inputs of flip-flops.

Recovering energy from internal nodes of flip-flops in a quasi-adiabatic fashion would also be desirable. However, storage elements of flip-flops cannot be energy recovering because we assume that they drive standard (non-adiabatic) logic. Due to slow rising/falling transitions of energy recovery signals, applying energy recovery techniques to internal nodes driving the storage elements can result in considerable short-circuit power within the storage element.

Taking these factors into consideration, we developed flip-flops that enable energy recovery from their clock input capacitance, while internal nodes and storage elements are powered by regular (constant) supply. Employing our flip-flops in system designs enables energy recovery from clock distribution networks and clock input capacitances of flip-flops.

The first proposed energy recovery flip-flop, Sense Amplifier Energy Recovery (SAER) flip-flop, is shown in Figure 3. This flip-flop, which is based on the sense amplifier flip-flop proposed in [4], is a dynamic flip-flop with precharge and evaluate phases of operation. In [5], this flip-flop is used to operate with a low-voltage-swing clock. We use this flip-flop to operate with an energy recovery clock. When the clock voltage exceeds the threshold voltage of the clock transistor (MN1), evaluation occurs. At the
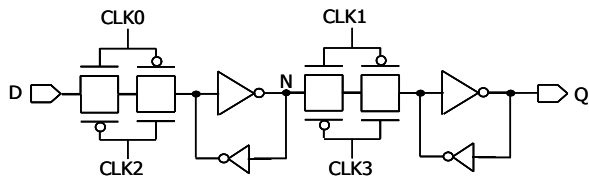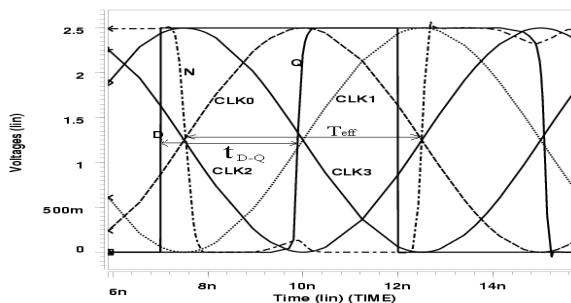
onset of evaluation, the difference between the differential data inputs (D and DB) is amplified and either SET or RESET switches to low and is captured by the set/reset latch. The SET and RESET nodes are precharged high when the clock voltage falls below V_{dd}-V_{tp}, where V_{tp} is the threshold voltage of the precharging transistors (MP1 and MP2).

Since the energy recovery clock has slow rising and falling transitions, there can be overlap between evaluation and precharge phases. This overlapping results in short-circuit current. In order to reduce the amount of this short-circuit current, the threshold voltages of the precharging transistors can be increased. In scaled dual-threshold voltage (dual-V_t) CMOS technologies, high-V_t devices can be used for the precharging transistors. Since our 0.25μm process (with 2.5V supply voltage) does not provide dual-V_t, we simulated a high-V_t PMOS transistor by adding a constant supply voltage of 0.386V in series with its gate terminal. This resulted in a 70% increase in the threshold voltage of the precharging transistors, which led to 17% power reduction. Figure 4 shows typical simulated waveforms of this flip-flop designed in a 0.25μm CMOS technology.

Although the SAER flip-flop is fast and uses fairly low power at high data switching activities, its main drawback is that either the SET or RESET node is always charged and discharged every cycle, regardless of the data activity. This leads to substantial power consumption at low data switching activities where the data is not changing frequently. We consider two approaches to address this problem. One approach is to use a static flip-flop, and the other is to employ conditional capturing [6].

Figure 5 shows the Static Differential Energy Recovery (SDER) flip-flop. This flip-flop is a static pulsed flip-flop similar to the Dual-rail Static Edge-Triggered Latch (DSETL) [7]. The energy recovery clock is applied to a minimum-sized inverter skewed for fast high-to-low transition. The clock signal and the inverter output
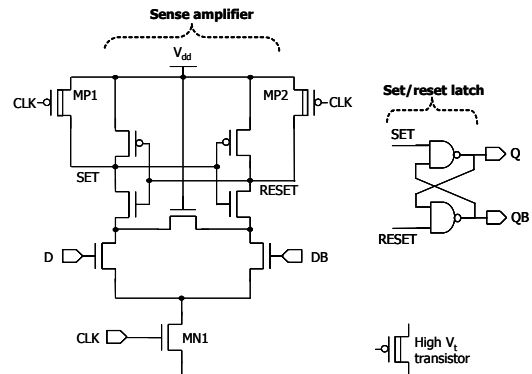

Fig. 1: Conventional Four-Phase Transmission-Gate (FPTG) energy recovery flip-flop [3]

Fig. 3: Sense Amplifier Energy Recovery (SAER) flip-flop

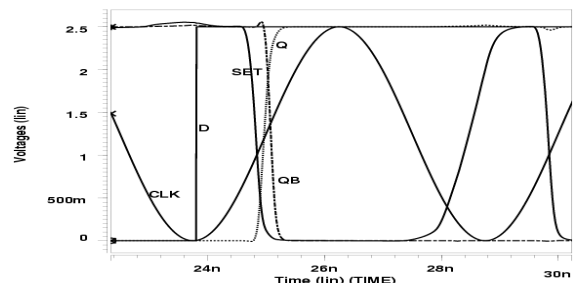**Fig. 2: Typical waveforms of FPTG flip-flop**

Fig. 4: Typical simulated waveforms of SAER flip-flop

(CLKB) are applied to transistors MN1 and MN2 (MN3 and MN4). The series combination of these transistors conducts for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltages above the threshold voltages of the NMOS transistors. Since the clock inverter is skewed for fast high-to-low transitions, the conducting period occurs only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB). However, due to the slow rising nature of the energy recovery clock, enough delay can be generated by a single inverter. Figure 6 shows typical simulated waveforms of the SDER flip-flop. In this flip-flop, when the state of the input data is the same as its state in the previous conduction phase, there are no internal transitions. Therefore, power consumption is minimized for low data switching activities.

The second approach for minimizing flip-flop power at low data switching activities is to use conditional capturing to eliminate redundant internal transitions. Figure 7 shows the Differential Conditional-Capturing Energy Recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a precharge and evaluate fashion. However, instead of using the clock for precharging, small pull-up PMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based Set/Reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output to control transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data is same as that of the output, SET and RESET are not discharged. Figure 8 shows typical simulated waveforms of the DCCER flip-flop.

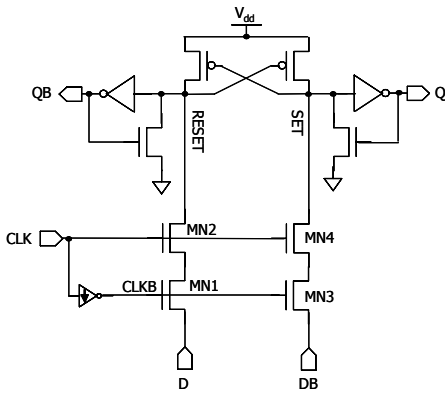As can be seen in Figure 8, CLK is generally less than Vdd/2

during a significant part of the conducting window. Therefore, a fairly large transistor is used for MN1. Moreover, since there are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become ON simultaneously. Having properly sized pull-up PMOS transistors (MP1 and MP2) instead of clock controlled precharge transistors ensures a constant path to V_{dd}, which helps to reduce the effect of charge sharing. Another property of the circuit that helps reduce charge sharing is that the clock transistor (MN1), which is the largest transistor in the
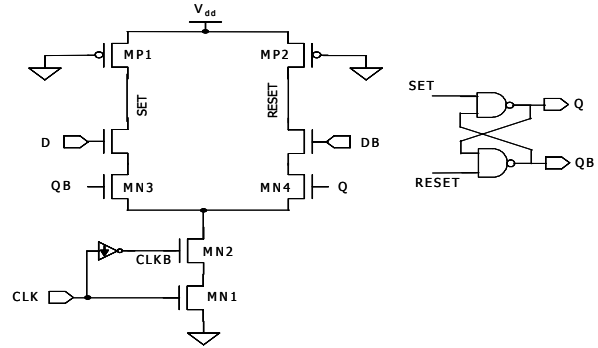

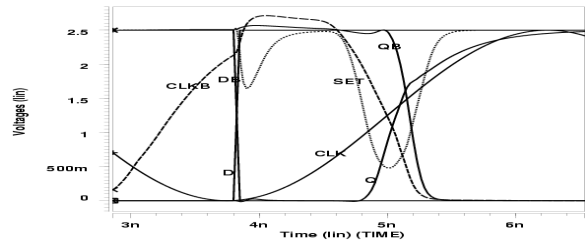**Fig. 7: Differential Conditional Capturing Energy Recovery (DCCER) flip-flop**

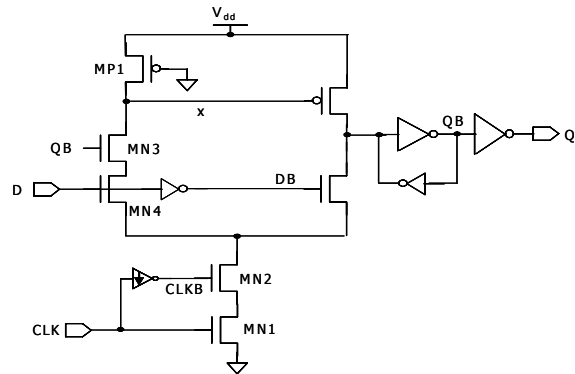**Fig. 8: Typical waveforms for DCCER flip-flop**

Fig. 9: Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop

Fig. 5: Static Differential Energy Recovery (SDER) flip-flop

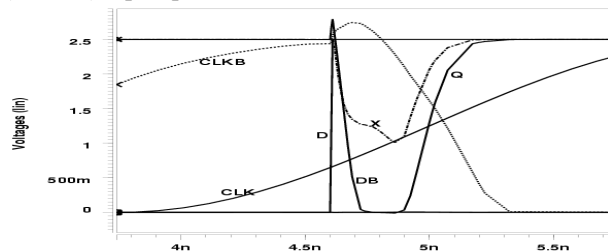**Fig. 6: Typical simulated waveforms of SDER flip-flop**

Fig. 10: Typical waveforms of SCCER flip-flop

evaluation path, is placed at the bottom of the stack. Therefore, the diffusion capacitance of the source terminal of MN1 is grounded and does not contribute to the charge sharing.

Figure 9 shows a Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flip. The transistor MN3, controlled by the output QB, provides conditional capturing. The right hand side evaluation path is static and does not require conditional capturing. Placing MN3 above MN4 in the stack reduces the charge sharing. That is because when the charge sharing occurs, the capacitance associated with MN3 is already charged and therefore does not contribute to the charge sharing. Typical simulated waveforms of the SCCER flip-flop are shown in Figure 10.

3. SIMULATION RESULTS AND COMPARISONS

All the flip-flops were designed and laid-out using TSMC 0.25μm process technology with a supply voltage of 2.5V. Netlists with parasitic capacitances were extracted from layouts and simulated using HSPICE. The designs were optimized at a temperature of 25°C for a clock frequency of 200MHz. However, since the FPTG flip-flop is a dual-edge triggered flip-flop, it was designed to operate at a clock frequency of 100MHz. A load capacitance of 30fF was used for all outputs. Figure 11 illustrates our timing definitions for energy recovery flip-flops. Delay is measured between 50% points of signal transitions. Setup time is the time from when data becomes stable to the rising transition of the clock. Hold time is the time from the rising transition of the clock to the earliest time that data may change after being sampled. Setup and hold times are measured with reference to the 50% point of the rising transition of the clock.

The proposed flip-flops are compared with the FPTG flip-flop. For individual flip-flop simulations, an ideal sinusoidal clock was used. Figure 12(a) shows clock-to-output (CLK-Q) delay and data-to-output (D-Q) delay vs. setup time for all the flip-flops. It is apparent that the delays of the FPTG flip-flop are much larger as compared to the proposed flip-flops. Figure 12(b) shows a clearer illustration of the behavior of the proposed flip-flops in the minimum delay region. For any flip-flop, there is an optimum setup-time that results in a minimum D-Q delay. This optimum setup time is near the minimum functional setup time and is used for comparisons of setup time. As shown in Figure 12, the CLK-Q delay becomes independent of setup time for long setup times. We use this value of CLK-Q delay for comparisons of CLK-Q delay. The SCCER flip-flop exhibits the smallest minimum D-Q delay, while the SAER flip-flop shows the smallest CLK-Q delay. The SDER flip-flop has the shortest setup time among the proposed flip-flops.

Figure 13 shows the dependence of D-Q and CLK-Q delays on clock frequency. Flip-flops are simulated from a frequency of 50MHz to their maximum frequency of operation. The flip-flops
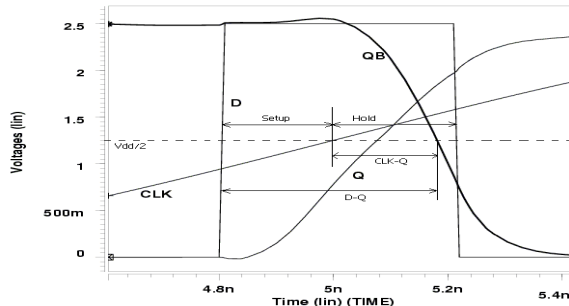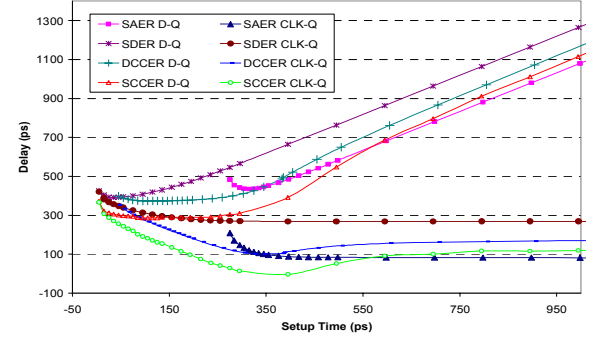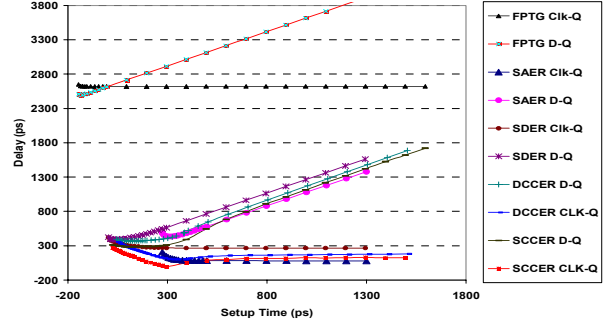

(a)

(b)

Fig. 12: Setup time vs. delay for (a) all flip-flops (b) proposed flip-flops
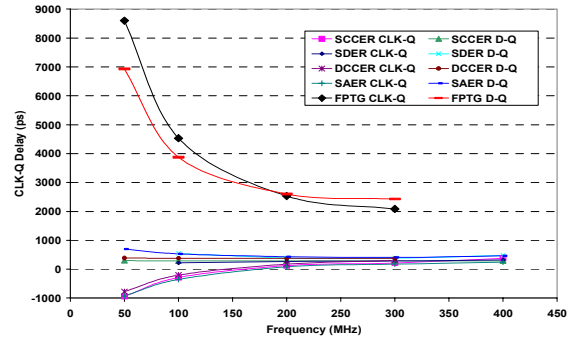

Fig. 13: Delay vs. Frequency for all flip-flops

were not re-optimized for each frequency. Although all the proposed flip-flops fail at frequencies above 400MHz, they can easily be re-sized to operate at higher frequencies. The proposed flip-flops show a higher range of operational frequency, and their delays are much less dependent on the clock frequency as compared to the FPTG flip-flop.

Figure 14 shows power as a function of data switching activity for different flip-flops. The SAER flip-flop has the lowest power consumption at high switching activities; however, it has the maximum power at low switching activities. The SDER and conditional capturing (DCCER and SCCER) flip-flops show less power consumption at low switching activities.

The SDER and conditional capturing flip-flops, however, consume more power than that of SAER flip-flop at high switching activities. This is because of the fact that at high switching activities there is much less opportunity for energy savings by using a static flip-flop or employing conditional capturing.

Figure 11: Sample waveforms illustrating timing definitions

	min D-Q delay (pS)	setup time (pS)	hold time (pS)	CLK-Q delay (pS)	Power* (μW)	PDP* (fJ)	Norm. PDP	Area (μm²)	Transist or count
FPTG	2491	-135[†]	740[†]	2619.7[†]	156.4	389.59	1	580.8	16
SDER	391.6	35	270	268.2	120.8	47.305	0.1214	133.9	14
SAER	434.8	355.3	-190	79.5	106.4	46.293	0.1188	139.2	18
DCCER	373.1	115.7	150	174.3	101.7	37.944	0.0974	136.9	18
SCCER	285.9	125	0	123.3	83.88	23.981	0.0616	196.8	17

*Power is for long setup time; Power-Delay-Product (PDP) is the product of this power and the minimum D-Q delay.
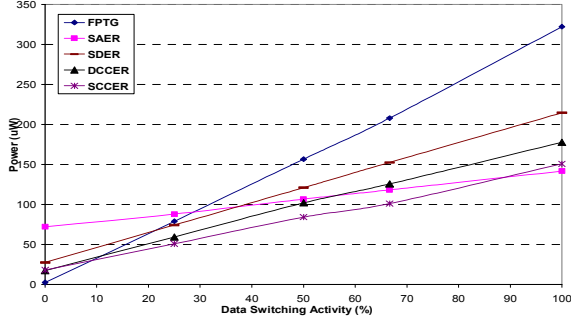
†As measured from the first phase clock (CLK0).

Fig.14: Power vs. data switching activity at 200MHz

Table 1 summarizes the numerical results for the flip-flops. The proposed flip-flops exhibit more than 80% delay reduction, a power reduction of up to 46%, and an area reduction of up to 77%, as compared to the FPTG flip-flop.

4. ENERGY RECOVERY CLOCKING

In order to demonstrate the feasibility of energy recovery clocking, we integrated 1024 energy recovery flip-flops distributed across an area of 4mm × 4mm and clocked them by a single-phase sinusoidal clock through an H-tree clocking network. The flips-flops were grouped into registers of 32 flip-flops, and the registers were evenly spaced in this area. A common data input was used for all flip-flops to easily control the data switching activity of the system. The clock was distributed using an H-tree network on the metal-5 layer, which has the smallest parasitic capacitance to the substrate. The width of the clock-tree interconnects was selected to be the maximum (35μm in our 0.25μm process) to minimize parasitic resistances. A lumped ∏-type RC model for each interconnect of the clock-tree was extracted and then connected together to make a distributed RC model of the clock-tree, as shown in Figure 15. The energy recovery clock generator drives the source node of the clock-tree (node CLK in Figure 15), and each final node
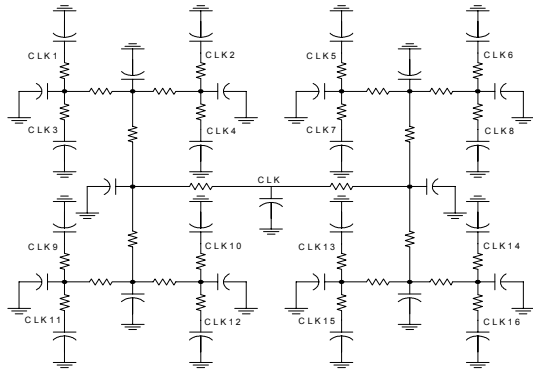
of the clock-tree (CLK1 to CLK16) is connected to two 32-bit registers.

The energy recovery clock generator is a single-phase resonant clock generator as shown in Figure 16(a). Transistor M1 receives a reference pulse to pull-down the clock signal to ground when the clock reaches its minimum; thereby maintaining the oscillation of the resonant circuit. This transistor is a fairly large transistor, and therefore, driven by a chain of progressively sized inverters. The natural oscillation frequency of this resonant clock driver is determined by:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

where C is the total capacitance connected to the clock-tree including parasitic capacitances of the clock-tree and gate capacitances associated with clock inputs of all flip-flops. In order to have an efficient clock generator, it is important that the frequency of the REF signal be the same as the natural oscillation frequency of the resonant circuit. In order to find the value of C, first with a given L and with the REF signal at zero, the whole system, including the flip-flops, is simulated. The clock signal shows a decaying oscillating waveform settling down to $V_{dd}/2$. From this waveform the natural decaying frequency is measured, and then by using Equation (1), the value of C is calculated. For the system with each proposed flip-flop, this experiment is carried out to determine the value of C. Having the value of C, the value of L for the frequency of 200MHz can again be determined from the Equation (1). The system consisting of the energy recovery clock generator, clock-tree, and flip-flops was simulated at the frequency of 200MHz (for all the proposed energy recovery flip-flops) with different data switching activities. Figure 17 shows a typical waveform of the generated energy recovery clock.

In order to compare with the square wave clocking, three flip-flops that operate with the square-wave clock were also designed. These flip-flops are Hybrid Latch Flip-Flop (HLFF) [8] and Conditional Capturing Flip-Flop (CCFF) [6], which are high-speed
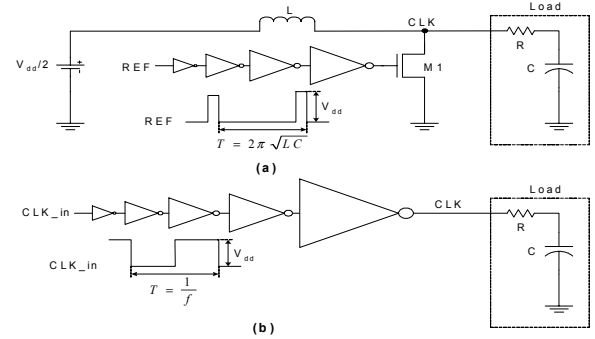

Fig 15: Distributed RC model of clock-tree

Fig. 16: (a) Resonant energy recovery clock generator (b) Non-energy recovery clock driver
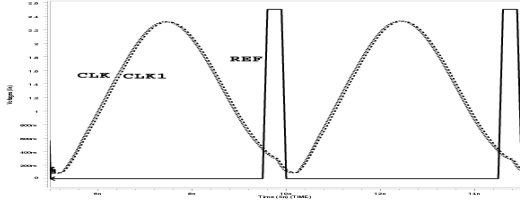
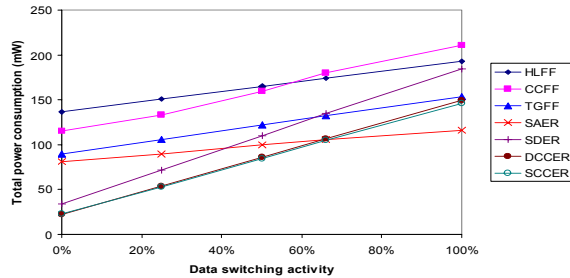**Fig 17: Typical waveform of generated energy recovering-clock signal**

Fig. 18: Total power vs. switching activity at 200MHz
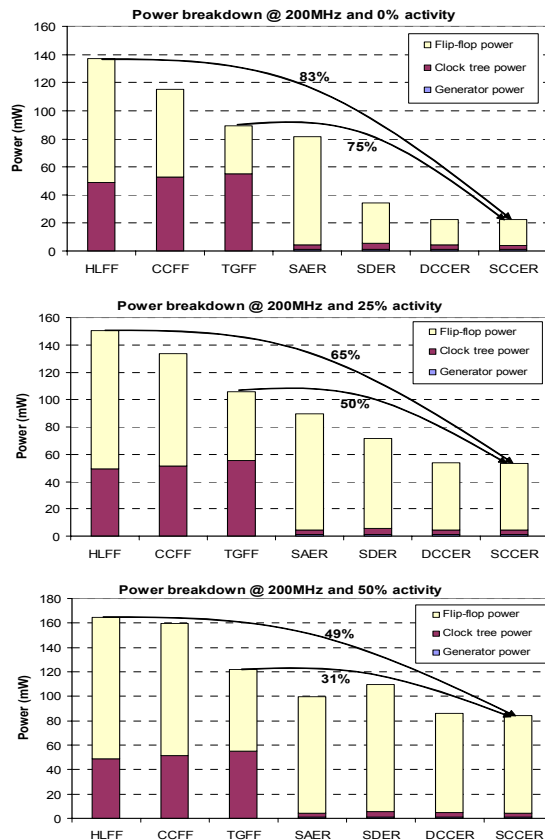

Fig 19: Power breakdown

flip-flops, and Transmission-Gate Flip-Flop (TGFF) [4], which is a low-power flip-flop. For square wave clocking, the clock-tree is driven by a chain of progressively sized inverters as shown in Fig 16 (b). The whole system of clock buffers, clock-tree, and flip-flops was simulated at a frequency of 200MHz with different data switching activities. Figure 18 shows the results of this experiment. The system power is plotted vs. data switching activity for the systems with different flip-flops. Among the square-wave flip-flops, the TGFF system shows the lowest power consumption for all

switching activities. The HLFF system has the highest power consumption at low switching activities, and the CCFF system shows the highest power consumption at high switching activities. Among the Energy Recovery flip-flops, the systems with conditional capturing flip-flops (DCCER and SCCER) exhibit the lowest power consumption at low switching activities (below 66%). For high switching activities, the system with SAER flip-flops has the minimum power consumption. The energy recovery systems show less power consumption at all switching activities as compared to the square-wave clocking, except for the energy recovery system with SDER flip-flops at switching activities above 66%. These results are similar to comparisons of individual flip-flops shown in Figure 14.

Figure 19 shows the power breakdown of the systems with different flip-flops at different switching activities. The energy recovery clocking scheme reduces the power due to clock distribution (clock-tree) by more than 90% compared to non-energy recovery (square-wave) clocking. The generator power overhead in the energy recovery scheme is very small, which indicates that the clock generator is very efficient. As compared to the HLFF system, the SCCER system shows power savings of 83%, 65%, and 49% at data switching activities of 0%, 25%, and 50%, respectively. When compared to the TGFF system (the lowest power square-wave system), the SCCER system shows power savings of 75%, 50%, and 31% at data switching activities of 0%, 25%, and 50%, respectively.

5. CONCLUSIONS

We proposed four novel energy recovery flip-flops that enable energy recovery from the clock network, resulting in significant total energy savings compared to the square-wave clocking. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. We implemented 1024 proposed energy recovery flip-flops through an H-tree clock network driven by a resonant clock-generator, generating a sinusoidal clock. Results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using conventional square-wave clocking scheme and flip-flops. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption.

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