The Flexible Processor
An Approach for Single-Chip Hardware Emulation by Dynamic Reconfiguration

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Abstract - A dynamically reconfigurable logic array, i.e., the Flexible Processor, suitable for a single chip emulation system is developed. It demonstrates the sequential execution of several sub-circuits divided temporally from an original large circuit. In order to accelerate emulation speed, a logic element, reducing total configuration data by 30% compared to conventional Look-Up-Table, and Temporal Communication Module (TCM) to support save/restore of circuit state and data communication among divided sub-circuits, are implemented on the Flexible Processor.

I. Introduction

We have developed a dynamically reconfigurable logic array, i.e. the Flexible Processor, suitable for a cost-effective single-chip digital circuit emulation system. Conventional emulation system employs a number of FPGAs in order to enhance the logic gate capacity, so that the system is very expensive. An emulation of large size circuit by using the Flexible Processor can be done by the following procedure. Firstly a logic-circuit to be emulated is divided into several sub-circuits by taking temporal data flow into account (temporal circuit partitioning) and each divided sub-circuit block is then implemented and activated sequentially using dynamic reconfigurability of the flexible processor. In order to realize such time-multiplexed programmable LSI, temporal data communication mechanism, which transfers temporal data from one sub-circuit to other sub-circuit at succeeding micro-cycles and user-cycle, is needed [1]. We have developed and implemented a Temporal Communication Module (TCM) for communication between user cycles and micro cycles, based on store/resume of flip-flop state in sub-circuits.

In dynamically reconfigurable FPGAs for single chip emulation, multiple configuration data must be all stored in the chip or downloaded from external memories. In order to increase the logic capacity and emulation speed, the reduction in configuration data size is needed. For this purpose, we have developed new logic element, with reduced configuration data amount, based on Full-Adder / D-flip-flop merged module (FDMM) [2].

II. Deisgn of the Flexible Processor

A. Logic Element

Fig. 1 shows the circuit diagram of the newly developed logic element. It is very different from conventional logic element using Look-up table (LUT), which is commonly used in today's FPGAs. We think LUT is too much redundant. A 4-input LUT, for example, can implement all possible 4-input logic functions (65536-kinds), but it requires 16-bit to configure and an application of logic-compaction algorithm in the technology mapping stage of logic synthesis procedure. In spite of its high functionality, frequently used logic functions are very limited (a few hundred kinds). Our 4-input logic element shown in Fig. 1 is composed by integrating FDMM and most frequently used three 4-input logic gates. FDMM can be configured as frequently-used 2- or 3-input logic functions by fixing some of inputs to 0 or 1. Two bits of configuration signal (SEL0, 1) select the output of modules. By using this logic element, the total configuration data to represent the same circuit, including routing configuration, is reduced by 30% as compared to LUT-based FPGAs [3].

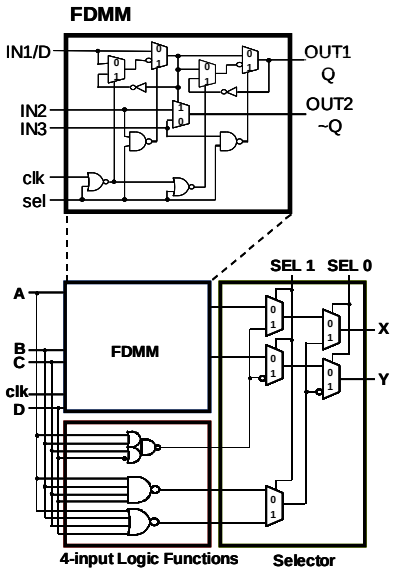

Fig. 1. Logic Element of the Flexible Processor

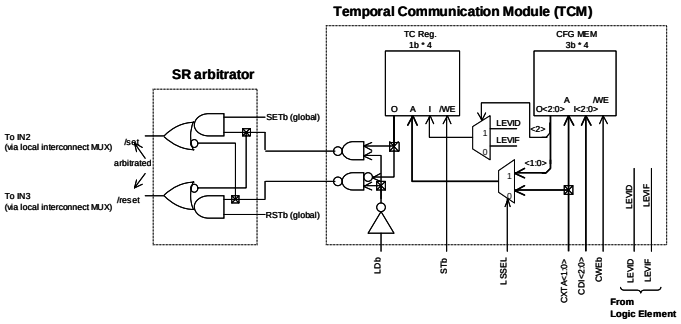

Fig. 2. Temporal Communication Module (TCM)

B. *Temporal Communication Module (TCM)*

Fig. 2 shows the block diagram of Temporal Communication Module (TCM). Four-plane 1-bit SRAM (micro register) is prepared to save the signal of each logic element. The input signal or the output signal of the logic element is stored into the micro register while the global store signal (STb) is active. One bit of configuration data determines take-in signal of input or output of the logic element. The write-back operation of circuit internal state is done by generating asynchronous set/reset signal (by SR-arbitrator) depending on the stored data and inputting to the logic element configured to flip-flop mode, while the global load signal (LDb) is active. LSSEL (Load / Store Select) signal determine the address of target micro-register, choosing from executing or destination address. Two bits of configuration data determine the destination address. In order to transmit the primary output of sub-circuit to the primary input of succeeding sub-circuit, the primary output of the sub-circuit is stored to TCM. Then the primary input of the succeeding sub-circuit is realized by inserting flip-flop to the succeeding sub-circuit as a primary input-pin.

III. Chip Test

The Flexible processor with on-chip 4-plane SRAM having a chip size of 3.9 x 3.9 mm^2 is fabricated using 0.6um CMOS technology. Table I and Fig. 3 show the summary and the chip micrograph. The measurement result of the chip is shown in Fig. 4: a 4-bit shift-register, partitioned into 4 micro-cycles, is working correctly by switching on-chip SRAM plane. The configuration data was generated by place and route software developed for the chip, and stored to on-chip memory prior to the execution. The fabricated flexible processor works 33MHz at 5.0V.

TABLE I
Summary of The Flexible Processor (FP-1)

Technology	CMOS 0.6um, 3-Metal, 1-Poly-Si
Chip Size	3.9mm x 3.9mm
Transistors	61k
Operation Speed	33MHz @ 5V (with context switch)
Context Planes	4
Logic Element	FDMM + 4-NAND, 4-NOR, AOI22A
# of LE	24 LE/CXT
Gate Capacity	240 logic gates/CXT (1LE = 10gate)
Effective Cap.	960 logic gates
User I/O	24 pin (4 bit/IOB x 6 IOB)
Configuration Data	30 bit/LE x 24LE = 720 bit 16bit/IOB x 6 IOB = 96 bit Total 816 bit (~34 bit/LE)
Configuration Cycle	30 cycle (32bit Configuration BUS width)

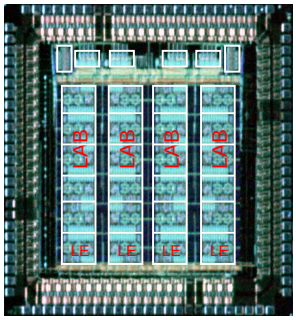

Fig. 3. Chip micrograph of the fabricated Flexible Processor (FP-1)

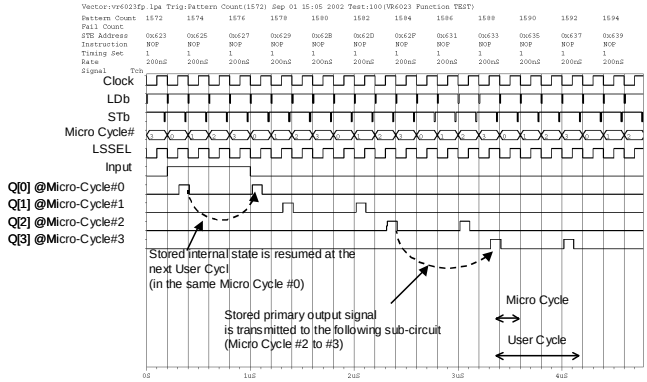

Fig. 4. Measurement result of the Flexible Processor, programmed as a 4-bit shift register

IV. Summary and Conclusions

We have developed a dynamically reconfigurable logic array, i.e., the Flexible Processor, suitable for a single chip emulation system. In order to improve the emulation speed, a logic ele ment is developed, which reduces the total configuration data by 30%, including routing configuration, compared to conventional Look-Up-Table (LUT). Temporal Communication Module (TCM) is also developed to support the communication between divided sub-circuits and the internal state save/resume. Finally the sequential execution of temporally divided circuit is demonstrated by fabricated reconfigurable logic array integrating the above components. The Flexible Processor with on-chip 4-plane SRAM fabricated by chip size of 3.9 x 3.9 mm^2, using 0.6um CMOS technology works 33MHz at 5.0V power supply.

Acknowledgements

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