Low Cost Analog Testing of RF Signal Paths

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Abstract

A low cost method for testing analog RF signal paths suitable for BIST implementation in a SoC environment is described. The method is based on the use of a simple and low-cost one-bit digitizer that enables the reuse of processor and memory resources available in the SoC, while incurring little analog area overhead. The proposed method also allows a constant load to be observed by the circuit, since no switches or muxes are needed for digitizing specific test points. Mathematical background and experimental results are presented in order to validate the test approach.

1. Introduction

The SoC approach to the design of electronic products allows rapid development of new products through reuse of basic design blocks or IP (intellectual property) cores [1]. Using this approach one can have a new functionality in the system by the addition of a new IP core. Thanks to market needs, the presence of wireless communication blocks to be embedded in systems-on-chip (SoC) is ever more present. Although the design time problem seems to be tackled by the IP reuse approach, the testability of such chips, especially for the high performance analog RF part, is still an open issue.

When discussing the testability of the overall system several difficulties arise, because of limited accessibility to the embedded blocks, and limited knowledge of third party designs. The use of BIST (built in self test) and accessibility schemes to the cores (like the P1500 [1] standard for digital cores) can help solve the test problem, mainly for digital circuits, where well known test strategies are available [2]. For analog and mixed-signal cores, however, test strategies are provided on a per circuit basis, and no general solution has been established [3]. Some BIST strategies have been proposed in an attempt to solve the testability problem of analog circuits: [4] for example, proposes an analog test core where a signal generator and AD converter are implemented for each analog block to be tested. An extension to the IEEE 1149.1 (1149.4- Standard for a mixed signal test bus) [5] makes use of an analog bus dedicated to test, trying to solve the accessibility problem.

The need for BIST structures for analog and RF circuits is increasing, as recent technology products require high-speed testers with analog and RF capabilities, thus increasing the test cost. One way to alleviate the test cost is to provide internal BIST structures that could be used to perform the test of specific parts, embedding the most demanding part of the analog tester on chip [6]. As the test of analog RF circuits is usually a specification-based test that should be performed at speed, incorporating structures that could ease the test and lower its cost would be desirable

Although there is a widespread use of wireless communications and portable devices, there are few methods in the literature that address BIST for analog RF signal paths. Current techniques are often based on some kind of loopback approach, in order to reuse the transmitter or receiver section [7,8,9]. While enabling some reuse, the reconfiguration required by these approaches is achieved through the use of switches and muxes that may degrade the performance of the circuit under normal operation, since non-linearities are introduced in the signal path. Also, the analog circuit will not observe a constant load - normal operation and test operation are performed on different circuits caused by the configuration mechanism, which makes the design of the analog circuit itself harder.

In this paper a low cost method for RF signal paths in a SoC environment is presented, which allows a significant reduction in the reconfiguration needed for the test and, at the same time, allows the reuse of processing and memory resources already available in the SoC. The method is based on the use of a one-bit digitizer that is permanently connected to the desired analog test point, thus minimally disturbing the circuit under test. Thanks to the simplicity of the converter, low analog area overhead is obtained, and high digitizing frequencies can be achieved. The implementation of the test is based on spectral analysis of the single-bit data acquired, being completely digital.

The paper is organized as follows: in section 2 a review of other approaches is presented. In section 3 the statistical sampler is presented. Section 4 presents an analysis of the RF signal path, discussing important points

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like linearity and IP3. In section 5 the proposed test approach is explained. Experimental results are presented in section 6, concerning a 100 MHz mixer and local oscillator pair. The paper finishes with analysis and conclusions in sections 7 and 8.

2. RF test techniques review

A strategy for the self-test of RF signal paths was suggested by [7], where a RF transceiver is tested using the AD converter of the system. The receiver path is tested first, and then the transmitter section is tested. This approach, however, is not able to observe specific test points in the signal path without switching the AD converter to that point. Another similar loopback strategy was proposed in [8] and, more recently, in [9]. One issue noted in loopback strategies is the possibility of specific faults being masked by the analog path used, since the entire RF signal path is tested and intermediate test points do not exist. For example, a defect in the transmitter could be masked by the use of an excellent receiver that filters the out-of-band distortion.

Recently, a signature test for RF integrated circuits [10] has been proposed, which applies a test signal to a DUT through an RF mixer, and captures the response by another RF mixer, thus allowing the application of special signals at the required speed. Reported results indicate that parameters related to linearity and noise can be observed by the approach. This approach, however, may not be suitable for BIST implementation, because of the additional resources needed, like mixers and AD converter. Other authors have focused on testability analysis of RF circuits in order to reduce overall system cost [11].

Since the loopback approach is not completely suited for BIST, and neither is the production test for RF circuits proposed in [10], a technique that has high fault coverage with the smallest possible performance degradation and area overhead is still to be developed. Taking advantage of low-cost samplers used in the test of linear devices [12], we propose the use of the statistical sampler as the BIST mechanism for embedded RF analog subsystems.

3. Statistical sampler

As several mixer parameters are estimated using spectral analysis, if one can observe spectral characteristics in some test points (like the output of the mixer), then a test strategy could be devised. In this section we propose the use of a sampler to implement such test.

In [12] a simple sampler was proposed, as shown in figure 1. It is composed by a voltage comparator and a white noise generator connected to one reference level. The input signal is connected directly to the input of the comparator. The digitized input signal is obtained at the output of the comparator and is a digital output.

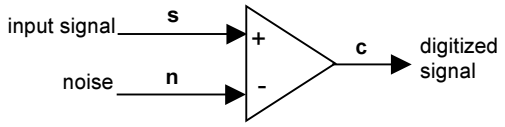

Figure 1. Statistical sampler.

The noise amplitude should be greater than or equal to the signal amplitude, and both signals should be zero mean (or have the same dc level). The autocorrelation at the output of the sampler, considering that the combined signal and noise is a normal stationary process with zero mean, is given by the arcsine law:

$$R_y(\tau) = \frac{2}{\pi} arcsin\left(\frac{R_x(\tau)}{R_x(0)}\right). \quad (1)$$

Equation (1) allows one to state that the statistics of the input signal will be at the output of the sampler, affected by a gain factor and by the arcsine function, which is approximately linear for small values of the input argument.

As the Fourier transform of the autocorrelation is the power spectrum density, one can note that this sampler allows the observation of the spectral characteristics of the signal, but with an increased noise level because of the addition of the noise at the comparator input (see [12] for details).

4. Analysis of an RF path

Mixers perform frequency translation by multiplying two signals, and are critical components in RF systems [13][14]. In a typical RF receiver stage (see figure 2), the antenna signal is amplified by a low noise amplifier (LNA) and after some filtering it is applied to a mixer. The mixer acts like a multiplier, and ideally it performs the product of the signal at the RF (radio frequency) input by the signal at the LO (local oscillator) input. The output of this operation is the IF (intermediate frequency) signal. If the RF and LO signals are sinusoids and the multiplier is ideal, the output of the mixer contains two frequency components: one at the sum ($f_{RF}+f_{LO}$) and other at the difference of the RF and LO frequencies ($f_{RF}-f_{LO}$).

The transmitter stage is similar to the receiver one, in the sense that it uses the same building blocks, but the mixer acts like an up-converter. In this case, a power amplifier is also needed. In the SoC environment, modern applications like the software-radio are strongly based on digital signal processing. Digital blocks with enough processing resources, together with AD and DA

converters are used to enable the implementation of the demodulation or modulation schemes.

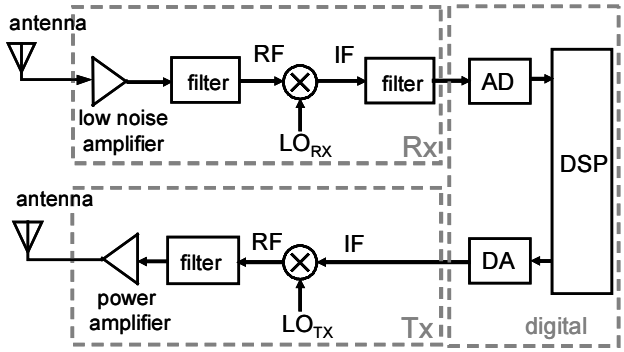

Figure 2. Generic transceiver system.

Being the initial stages in the reception, the performance of the LNA and the mixer directly affect the performance of the entire receiver. The most important parameters are related to noise and linearity characteristics. These performance requirements are expressed using special parameters, like those listed in table 1 (from [13]).

Table 1. Typical mixer characteristics.

Noise Figure (NF)	12 dB
Input third-order Intersect Point (IIP_3)	5 dBm
Gain	10 dB
Port-to-Port Isolation	10-20 dB

The noise figure is a measure of how much the signal to noise ratio (SNR) degrades as the signal passes through a RF stage. The intersect point is a measure of intermodulation distortion caused by a non-linearity in the signal path. The third order intersect point characterizes a 3rd order non-linear distortion. The IIP3 is measured in a two-tone test [13] [15] (where the amplitudes of the tones are the same and known), by measuring the attenuation of the intermodulation products with respect to the desired IF outputs, as shown in figure 3. One can observe that the measurement procedure is based on spectral analysis of the output of the mixer. In figure 3, signals at frequencies w1 and w2 are the desired IF outputs, and signals at frequencies (2*w1-w2) and (2*w2-w1) are the undesired intermodulation products. The measurement of IP3 is usually done by the use of two signal generators (one for each frequency) and the measurement of the output using a spectrum analyzer (for example, see [16]).

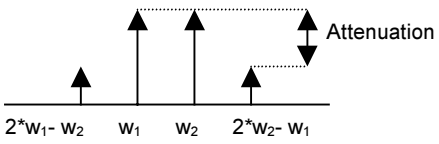

Figure. 3. Attenuation measurement for intersect point evaluation.

5. Test Method

The proposed test method is based on the evaluation of the spectrum at specific test points in the analog signal path, as illustrated in figure 4. Memory and processing resources from the SoC environment could be used in order to implement the test. As the output of the sampler is a digital signal, it can be interfaced directly to the digital part of the system through a data bus.

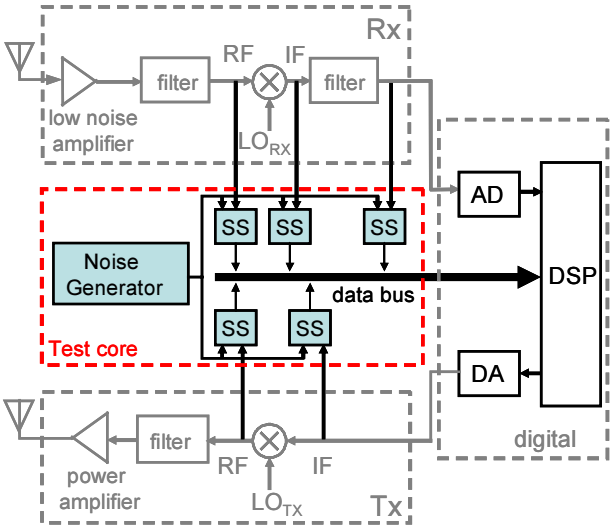

Figure 4. Generic transceiver system with testing capabilities.

5.1 Test example using Matlab simulation

In order to illustrate the proposed approach, a simulation for a two-tone test was run in Matlab using a behavioral model for the mixer, which allows the fine-tuning of third-order distortion ([14]). Two tests were executed with different values of IP3, so one would expect to observe different levels of distortion.

The simulations considered an input signal with two tones, and a sinusoidal signal at the LO input. The spectrum of the IF signal was evaluated using a single FFT of the entire signal. In figure 5, the spectrum of the IF signal observed through the proposed sampler is also shown. One can observe that the noise floor has significantly raised, and completely hides the intermodulation products, but the main components are clearly visible.

If the OIP3 is decreased from 10dBm to -3dBm, while the remaining parameters are held constant, the intermodulation products now become as shown in figure 6. One can see that the intermodulation terms are

clearly visible in the spectrum evaluated from the sampler output.

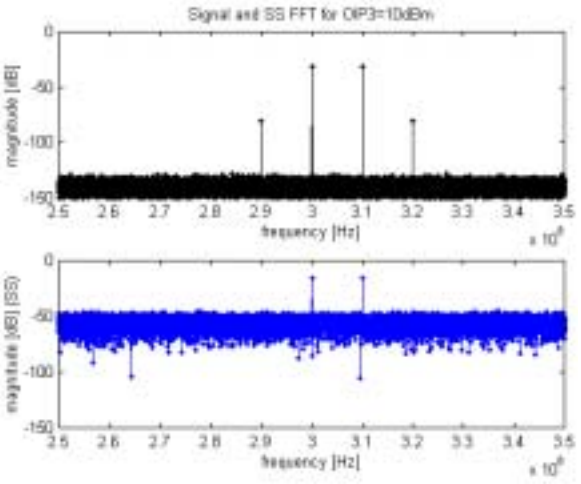

Figure 5. IF Spectrum with infinite resolution converter and spectrum obtained from sampler

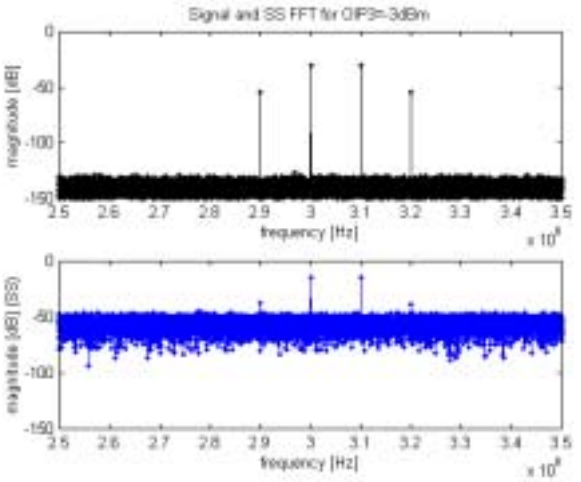

Figure 6. IF Spectrum with infinite resolution and spectrum obtained from sampler for a large distortion

6. Experimental results

In this section we address implementation issues by prototyping a single-balanced active mixer in real hardware. The first implementation is at low frequency and contains the mixer block and an active low pass filter. It illustrates the insertion of faults in the filter and the variation of the bias voltage influencing the third-order intermodulation products. The second implementation addresses a relatively high frequency.

6.1 Testing a mixer and filter

The setup in figure 7 has been prototyped using a CD4007 device (for implementing a single-balanced active mixer) and a programmable low pass filter. Two-tone signals were applied at 60 and 63 kHz. The local oscillator frequency was set to 50 kHz. Statistical samplers were used in each one of the differential signals at the output of the mixer and at the output of the filter.

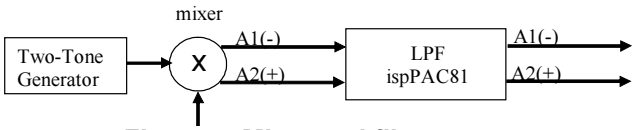

Figure 7. Mixer and filter setup

For a bias voltage of 3.3V one obtain the results shown in figure 8. In the lower trace it is shown the spectra observed through the statistical samplers. The large tone at 50 kHz dominates the spectra. As the noise floor is related to the maximum signal level, the intermodulation tones of the demodulated mixer signal at 7 and 16 kHz are completely masked.

In the upper trace it is shown the spectra after low-pass filtering. The 4th order filter has a cutoff frequency of 30.1 kHz. As the amplitude of the local oscillator has been reduced, the intermodulation terms are clearly visible and cound be used in order to estimate the third order distortion.

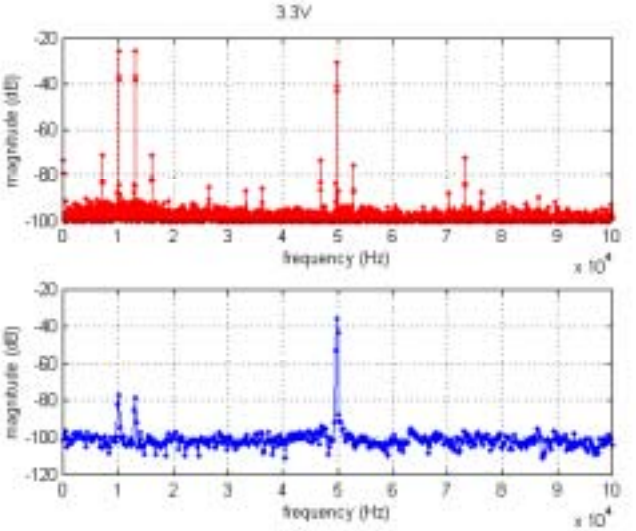

Figure 8. Spectra at the mixer output (lower) and filter output (upper)

If one now changes the bias voltage of the mixer to 3.0V the intermodulation terms change, as could be verified in the upper plot of figure 9. If one goes further and changes the filter cutoff frequency to 35.6kHz the results shown in the lower trace of figure 9 indicate a significant increase in the local oscillator magnitude, as

the filter attenuation is greatly reduced at the oscillator frequency.

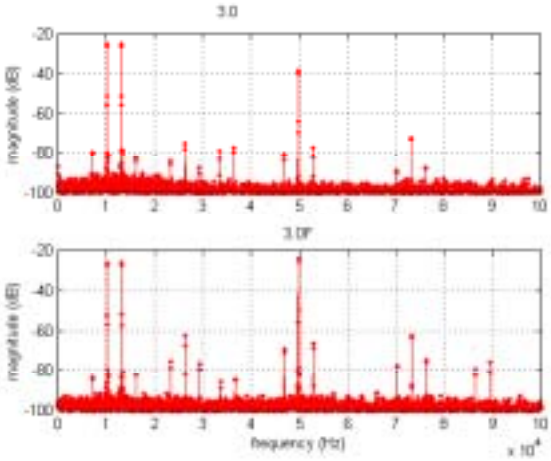

Figure 9. Spectra at the mixer output for 3.0V(upper) and for different filter (lower)

6.2 Testing a mixer at 100MHz

In order to verify the applicability of the approach to more realistic circuits, a prototype mixer and a local oscillator circuit running at 100MHz were built using discrete RF components (see figure 10). Fast voltage comparators (2.5ns propagation delay) were used to implement the statistical sampler, allowing the observation of the signals at the output of the mixer. A logic analyzer was connected to the comparators output in order to acquire the resulting bitstream. Data was transferred to a PC and analyzed using Matlab. The block diagram of the measurement setup is shown in figure 11.

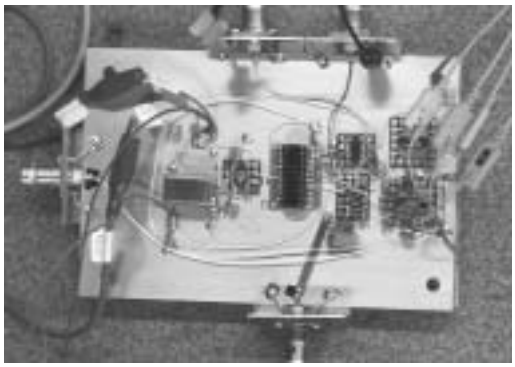

Figure 10. Prototyped mixer board

After applying two tones at 101.00 MHz and 101.06 MHz, diverse harmonics are expected at the output of the mixer. This is confirmed by the output of the spectrum analyzer in figure 12.

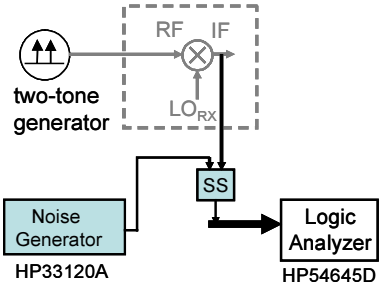

Figure 11. Block diagram of experimental setup

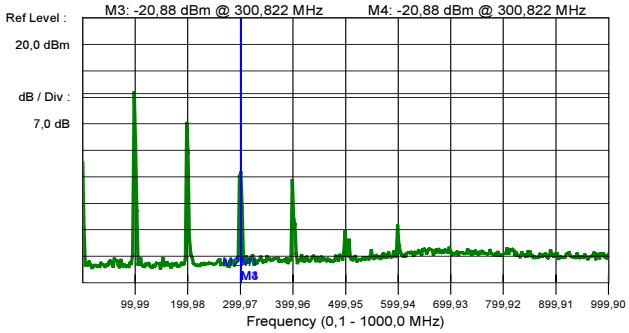

Figure 12. Spectral analysis of mixer output

As the local oscillator is running at 100MHz, the two-tones should be down-converted to the 1.00MHz and 1.06MHz bands. The results of observing this frequency band using the spectrum analyzer are presented in figure 13. The large intermodulation distortion components were already present in the original input signal to the mixer.

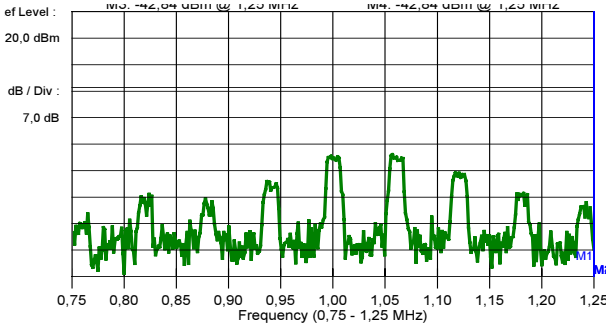

Figure 13. Spectral analysis of mixer output

The same frequency band was analyzed using the output of the comparators and produced the results shown in figure 14. This figure also shows results after changing the bias voltage of the active mixer, simulating a parametric fault. One can clearly distinguish the two traces in figure 14, confirming that the use of the statistical sampler to probe non-linear circuits is a valid test approach.

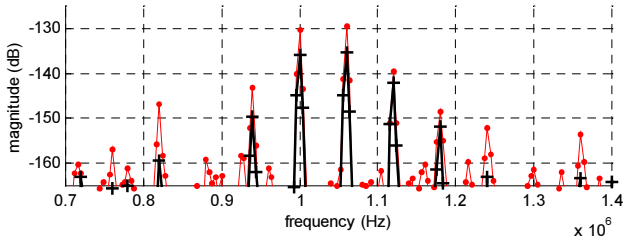

Figure 14. Spectral analysis of mixer output

7. Analysis

The insertion of low cost sampler in the RF path has key advantages when compared to a loopback approach: less reconfigurability, constant loading for the analog circuit, an increase in observation and circuit partitioning capabilities.

Simulation and practical results have shown that it is possible to use the approach to verify spectral dependent parameters like IP3. The use of a voltage comparator as a 1-bit sampler enables the construction of high speed acquisition systems, making it more realistic to sample signals at IF and RF. Another advantage is that sub-sampling techniques can be used with this sampler, and could be used in a way to provide a signature for the mixer and other blocks (see [17]).

The analog noise generator needed for the samplers can be realized with little analog overhead (see [18]), as only one generator is needed for all samplers. One issue is that the amplitude of the noise should be greater than or equal to the amplitude of the signal being measured, at each test point.

The application of the test signal has not been addressed yet, and should be provided by a stand-alone generator (like the one proposed in [7]), or by deviating the transmitter signal to the receiver using some kind of loopback technique. The main advantage of the proposed test technique over loopback is the increased observation capability enabled by the use of the sampler. This approach would be able to detect a faulty transmitter that outputs a tone at an out-of-band frequency, for example.

8. Conclusions

This paper has presented a first approach for low cost BIST of RF sensitive analog parts, based on the statistical sampler approach. Mathematical background and experimental results have shown the validity of the approach. Presently, we are working in the characterization of the technique and its application to other RF blocks like frequency synthesizers.

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