Leakage Current Reduction by New Technique in Standby Mode

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ABSTRACT:

In this paper, a new approach for reducing the subthreshold leakage current of digital circuits is proposed. It does not use a multi-threshold process technique which is more expensive. The technique which makes to use of a new variable supply voltage oscillator, combines the ideas of both Standby Leakage Control Using Transistor Stacks (SRB) and variable threshold (VT) methods. In this technique compared to the Leakage Control Using Transistor Stacks method, the subthreshold current decreases three times. In addition, leakage current monitor (LCM) and its related circuits which are used in VT techniques are not required here. This makes the proposed technique more power and area efficient.

Categories and Subject Descriptors:

B.7.1 [**Hardware**]: Integrated Circuits - *type and design style*

General Terms: Design.

Keywords: Digital Integrated Circuits, Subthreshold Current, Leakage Current, Low Power, Static Power.

1. INTRODUCTION

In digital circuits, there are two types of power consumptions which are dynamic and static power dissipations. The dynamic power dissipation includes the switching power and the short circuit power consumption. This component of the power is consumed during the switching of the nodes between high and low voltages. The static power is mostly due to subthreshold leakage current. This current, although is very small, when compared to above threshold, but leads to a considerable power consumption in VLSI circuits because of the very large number of transistors.

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During the standby mode of the operation, the subthreshold power consumption is the most important component. For a circuit, with the time in active mode less than 10% [1] of the total time, this component becomes vital. This current is related to the input voltage with the following exponential relation [2]:

$$I_{sub} = \frac{W}{W_0} I_0 \, e^{\frac{(V_{gs}-V_t)}{nV_{th}}} = \frac{W}{W_0} I_0 \, 10^{\frac{(V_{gs}-V_t)}{S}} \qquad (1)$$

Here I_{sub} is the subthreshold current, W is the transistor width, I_0 and W_0 are the subthreshold current and transistor width for the reference transistor, V_{th} is thermal voltage, n is a constant, V_t is the threshold voltage, V_{gs} is the gate-source voltage, and s is the subthreshold slope.

The objective of this paper is to present a technique for subthreshold current reduction in digital circuits. In Section 2, main approaches reported in the literature for reducing the subthreshold current in Standby mode are briefly described while in Section 3 our proposed technique is presented and compared to the previous methods. The simulation results are presented in Section 4 and finally the summary and the conclusion are given in Section 5

2. SUBTHRESHOLD LEAKAGE CURRENT REDUCTION TECHNIQUES

There have been several techniques to reduce the static power due to the subthreshold leakage current (see, e.g., [1]-[5]). Using some of these methods, the static power dissipation can be reduced up to four orders of magnitude [1].

2.1 Self-Reverse Bias (SRB)

This method, which is schematically shown in Figure 1, is one of the important approaches in reducing the subthreshold leakage current during Standby mode. Here, one transistor which is in series with the digital block, V_{DD} or *GND* or both are disconnected from circuit during Standby mode. Therefore, the subthreshold current is reduced nearly four

orders of magnitude. The use of this technique is limited to combinational circuits.
To minimize this effect, the size of this transistor should be maximized to a level such that it does not add too much parasitic capacitance, destroy the operation of circuit, and increase the subthreshold leakage current of this transistor.

2.2 Multi Threshold (MT)

This method is a modified version of the SRB technique. In this approach, the transistor which disconnects V_{DD} or *GND* from main circuit has high V_t and the logic transistors have low V_t (see Figure 2).

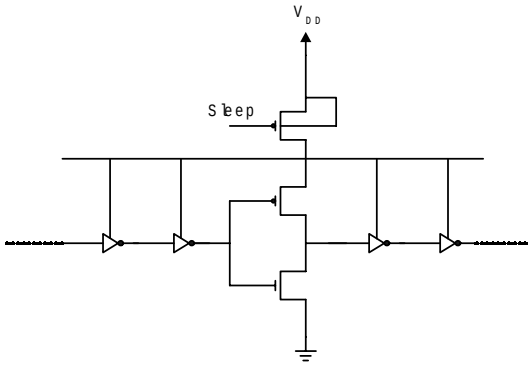

Figure 1. Self Reverse Bias Technique. [3]

The main problem with this technique is the existence of an extra step in process flow that increases the cost. There are also SRB problems, in this approach [4] .

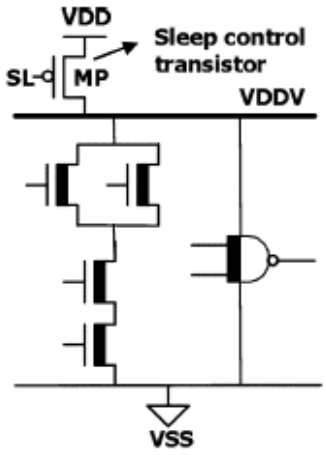

Figure 2. Multi-Threshold (MT) Technique [1]

2.3 Super Cut-off CMOS (SCCMOS)

This technique has been proposed to solve the problem of the extra cost of the MT approach. The basic idea behind this method is to turn off completely the transistor which connects the main circuit to V_{DD} or *GND*. This is achieved by connecting the gate of the transistor to a voltage which is higher than V_{DD}. This leads to a positive V_{gs} for a PMOS transistor (see Figure 3) and, hence, the sub threshold current reduces exponentially with increasing this voltage. The increase in the gate voltage is obtained using a charge pump circuit which is shown in Figure 4.

2.4 Variable Threshold (VT)

This technique makes use of the body effect which implies that the threshold voltage is changed by the bulk voltage (V_{BB}). Therefore, varying this voltage, in standby mode, one can increase V_t reducing the sub threshold current exponentially in this mode. During active more, the body voltage is the same as the source and hence reducing the threshold voltage to the value without the body effect increase (see Figure 5.). Here, no extra transistor is required for separating V_{DD} from the main logic circuit. The benefit of this approach compared to the previous methods is that we can use it in sequential circuits as well. This is due to the fact that the voltage levels remain unchanged in the standby mode.

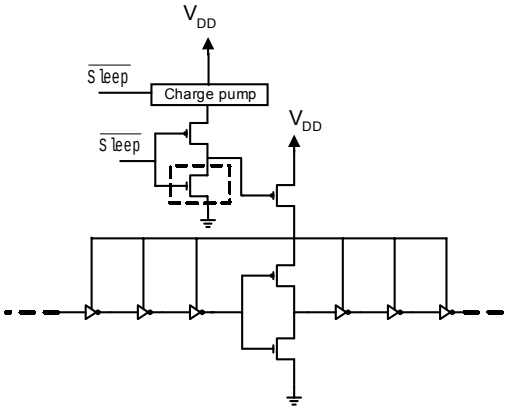

Figure 3. Super Cutoff MOS technique [2]. For example, the number of NOT gates in the main logic circuits can be one thousands here.

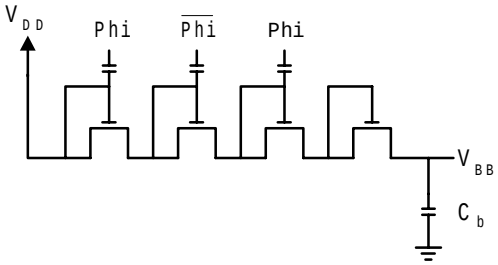

Figure 4. Charge pump circuit [1], [2], [5]. Phi is the output voltage of the oscillator.

This extra power consumption is the main drawback of the method [5]. There have been reported approaches which use the body effect to reduce the power in standby. Some of the approaches include SPR w/SSB [2], and SAT+SPR (self adjusting threshold voltage) [1]. The techniques in [1] and [2] do not require any supply voltage different than the circuit supply voltage. The operation principles of both approaches are almost the same in standby mode. Here, using a charge pump (see Figure 4), an oscillator and an LCM (leakage current monitor) circuit the bulk voltage level changes [1], [2]. There are some drawbacks for these two methods: First, the sub threshold leakage current reduction is not as much as those of MT and SRB methods. Second, the existence of an oscillator in these circuits itself leads to some considerable power consumptions due to fact that the pump circuit in these techniques should charge a large capacitance which is the sum of the parallel bulk capacitances of all gates. Also, in the technique of [2], there is a leakage current during the sensing

of the bulk voltage by the LCM circuit. In addition to this leakage, there is another leakage current flowing through the switch during standby mode. This leakage current passes through the off transistor at the output of the charge pump circuit (similar to the SCCMOS technique).

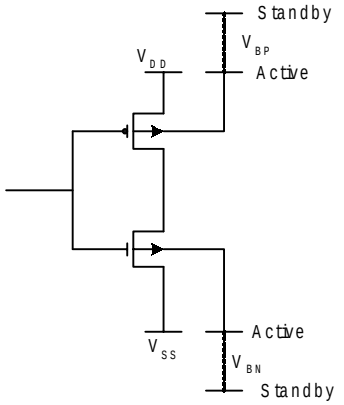

Figure 5. VT Technique in [1], [2].

These sub threshold currents increase the power dissipation of charge-pump. Finally, the LCM circuit of [1] occupies a rather large area (use a transistor with a very large width) which can be considered as another disadvantage.

3. PROPOSED TECHNIQUE

This method combines the ideas behind the SRB and the VT methods. Similar to the SRB method, during standby mode, one transistor is utilized to separate V_{DD} from the logic circuit. In addition, to reduce the subthreshold current, the VT method is used to increase V_t. The power reduction in this technique is better than that of the SRB method while not having the problems of the MT approach. (see Figure 6). In this figure, the circuit which is used to increase V_t is SSB (Self Reverse Bias). It includes a charge pump circuit and a new oscillator. Because the charge pump should deal only with one transistor here, the bulk capacitance of this transistor is small requiring a weak oscillator circuit compared to the VT method. In the proposed approach, we invoke a new oscillator circuit enabling us to avoid the switch used in [2] which connects the bulk voltage to V_{DD}. Hence, the switch leakage current during standby mode is omitted. Consequently, the charge pump circuit can operate with a low power in this mode. This oscillator circuit, which is shown in Figure 7, sinks only a current of 15nA for a 70nm CMOS technology and a 0.7V supply voltage [6]. This circuit is the same as the conventional oscillator with this difference that its power supplies during each mode of operation.

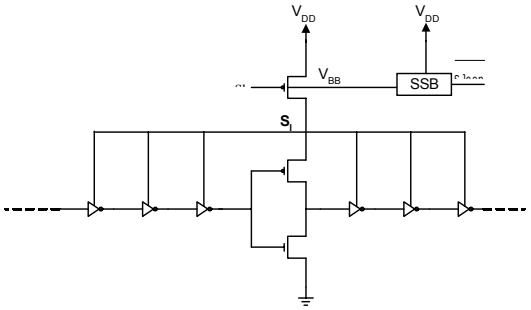

Figure 6. Main circuit used for simulations.

In standby mode, there are two diode connected transistors in the power path and hence the supply voltage of the oscillator can reduce to 0.2V and in active mode there exist four diode connected transistors in the path making the oscillator supply voltage equal to 0.08V. Because, the supply voltages for this oscillator are low in both modes, all transistors of the charge pump circuits can operate in the sub threshold region consuming a minimum power. In addition, this approach does not require an LCM circuit and its related circuits. The reason for this is that the charge pump oscillator does not need to be turned on and off for its low power dissipation. The output of the oscillator for both standby and active modes is shown in Figure 8. In the reduced power supply mode, both the amplitude and oscillating frequency is decreased which leads to a reduced bulk voltage. The bulk voltage in both modes is shown in Figure 9. As can be observed from this figure, the bulk voltage does not exceed the reverse break down voltage of the bulk-drain junction. In addition, the charge pump is strong enough to raise the bulk voltage to the level of substantially reducing the sub threshold leakage power. The bulk voltage which is the voltage of the parasitic capacitance of the cut-off transistor, raise to a high level so that the pulled leakage current of p-n junction is equal to pushed current with the charge pump circuit.

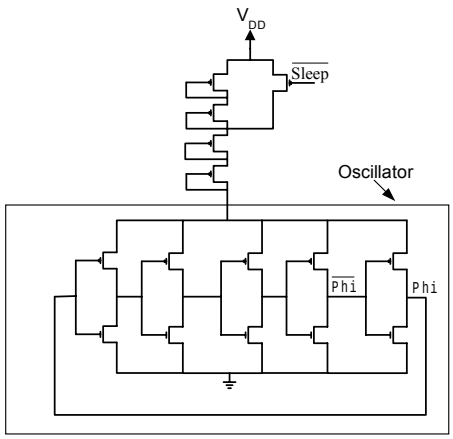

Figure 7. The oscillator circuit that used in this approach.

This keeps the bulk voltage constant. Therefore, the amount of charge pump is in the acceptable range for both modes.

4. SIMULATION RESULTS

As previously mentioned, because of using both the SRB and the VT approach, one can expect that the static power consumption is lower than that of each of the approaches individually. The static power saving of VT is smaller than that of SRB because in SRB, the number of off transistors is more than that of VT.

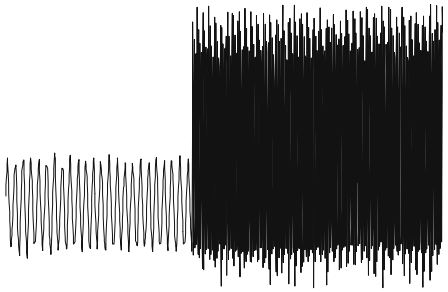

Figure 8. Variation of oscillation frequency and voltage level (power) in two operating modes. Phi is the output voltage of the oscillator circuit.

Therefore, if the proposed approach can reduce the static power consumption more than SRB, the new approach will lead to a lower static power dissipation than both VT and SRB. The SPICE simulated results for an array of 1000 NOT gate is presented in Table I. The reason that we have utilized NOT gates is that they consumes the largest static power owing to the fact the number of off transistors in series is the least. As is evident from the results, the power is three times smaller compared to that of SRB. Also, it should be mentioned that the charge pump circuit consumes 100μA in VT for a technology of 0.35μm (control circuit excluded) [1]. The corresponding circuit uses 20nA in the proposed approach leading to 5×10^3 times less current in a technology of 70nm.

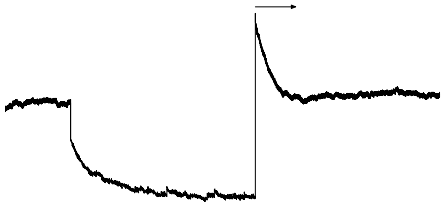

Figure 9. Bulk voltage in active and standby modes for the transistor which connect V_{DD} to the main circuit, The power supply voltage that is used in the result was 0.7 V.

The transition time from active mode to stand by mode is 20μs (Figure 9) that is shorter than corresponding times in [2], [1]. Transition time from standby to active mode is as short as the times in [2], [1]. Figure 10 shows the virtual power which is the voltage of node S_l of circuit Figure 6.

5. SUMMERY AND CONCLUSION

A new technique for reducing the subthreshold leakage current of digital circuits was proposed. It combined the ideas of both the SRB and VT methods. It made use of a new variable supply voltage oscillator to eliminate the LCM and its related circuits. This made the technique more power and area efficient. In addition, since the proposed technique does not need multi-threshold process, it is a cheaper and hence preferable.

Table I. Results of static power dissipations for the proposed structure, SRB and SCCMOS.

Technique / Block	This Work	SRB	SCCMOS
Charge pump	16.5nw	__	5μw
Main structure	12nw	36nw	2nw

The SPICE simulation results were presented for an array of 1000 NOT gates. Three times less power dissipation was obtained when compared to that of the SRB method.

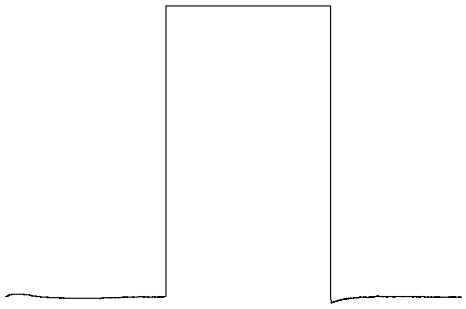

Figure 10. Voltage variation of the virtual power node in active and standby modes.

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