Estimating Detection Probability of Interconnect Opens using Stuck-at Tests

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ABSTRACT

An interconnect break is a break that occurs in the interconnect wiring, which results in logic gate inputs being disconnected from the drivers and causes the wire to float. Interconnect breaks are the most common types of breaks in modern $CMOS$ integrated circuits, so testing and detecting these breaks has become very important. This paper proposes a model by which standard tests for stuck-at-faults can be used to detect interconnect breaks in a circuit. We do a worst-case analysis of the detection of these breaks and calculate the minimum number of test vectors required to detect breaks with a specified confidence level, using n-detection principles. To enhance the understanding of the breaks in the circuit, we present a statistical model based on the length distribution of the wires surrounding the floating wire where the break occurs. From the model we compute the detection probabilities of such breaks and show that the worst case of detection is when the bias voltage is the same as the logic threshold voltage.

Categories and Subject Descriptors: B.8.1 [**Logic Design**]: Reliability, Testing and Fault-Tolerance

General Terms: Reliability

Keywords: Break fault, interconnect open, stuck-at test

1. INTRODUCTION

The three classes of defects that can occur during the manufacturing process of an integrated circuit (IC) are bridge defects, break (open circuit) defects, and parametric delay defects [4]. This paper is concerned with defects of the second type (i.e., *breaks*). They are caused by breaks in the conducting material of a circuit layout due to spot defects, either by lithography-related errors [8], masking errors or fabrication errors. Based on their locations in different parts of a circuit, breaks can be categorized as: (1) *interconnect break*, which occurs in the interconnect wiring, resulting in logic gate inputs being disconnected from their drivers and causing the wire to float, (2) *network break*, which occurs inside a CMOS cell, affecting the connection between the transistor drain and source, (3) a break inside a CMOS cell that can affect the connection between the bulk of a n-channel transistor and *Gnd*, or the bulk of a p-channel transistor and V_{dd}, and (4) a break that can disconnect a single transistor gate and its driver [12, 2, 6].

In modern ICs, as the number of layers of metal have increased so has the interconnect wiring, which results in a higher probability of interconnect breaks. The number of vias far exceed the number of transistors and these vias are particularly susceptible to opens [16]. This makes testing and detection of interconnect breaks all the more important. This paper addresses interconnect breaks.

Konuk [6] described a fault simulation algorithm for detecting interconnect opens. Konuk's algorithm took into account the capacitance between the floating wire (FW) and surrounding wires, Miller (gate/drain, gate/source) capacitances to the FW, charge collector diodes, and trapped charge deposited on the FW during fabrication. These factors are used by his algorithm to calculate trapped charge intervals on the FW, for a set of stuck-at tests. The fault simulation algorithm computes the maximum trapped charge on the FW with which the given test set can detect the open as a stuck-at-0 fault (*i.e.* $Q_{max,sa0}$), and the minimum trapped charge on the FW with which the given test set can detect the open as a s-a-1 fault (*i.e.* $Q_{min,sa1}$). If the fault simulator determines that $Q_{max,sa0} > Q_{min,sa1}$, then the interconnect break would have been detected and the fault dropped.

Konuk deals with the detection intervals for trapped charge, but mentions that it would be ideal to consider the detection probabilities instead. Konuk's fault simulator required knowing the logic value on each wire adjacent to the FW. This paper presents a method that uses the probability of detecting interconnect breaks while applying randomly selected n stuck-at-zero and n stuck-at-one tests for each fault location in the circuit, and proposes a statistical model that uses the length distribution of the surrounding wires instead of their logic values. Length distributions estimates of in-

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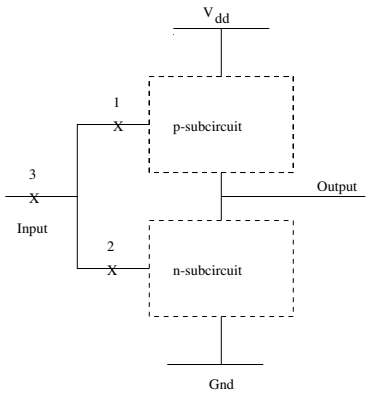

Figure 1: A symbolic CMOS circuit showing the location of the three possible classes of interconnect opens.

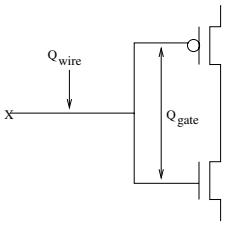

Figure 2: Figure showing distribution of charge

terconnect wiring are often available from the circuit design of modern VLSI circuits [3, 14], which our approach can use directly.

As mentioned earlier, interconnect opens cause floating gates. Such opens can be categorized as: (1) opens that cause floating gates affecting only the subcircuit consisting of p-transistors (p-subcircuit), annotated as 1 in Figure 1, (2) opens that cause floating gates affecting only the subcircuit consisting of n-transistors (n-subcircuit), annotated as 2 in Figure 1, or (3) opens that cause floating gates affecting both the p-subcircuit and the n-subcircuit, annotated as 3 in Figure 1 [18].

Maly [9] observed that an interconnect open affecting either the p-subcircuit or the n-subcircuit does not hinder the functional behavior of the circuit, except for some changes in the circuit delay. However, an open affecting both the p-subcircuit and the n-subcircuit affects the whole charging and discharging path between the ground and V_{dd} planes and thus changes the logic function of the circuit. Furthermore, since the wiring length is so great, type 3 open defects are by far the most common. Therefore, in this paper we consider the latter type of interconnect open, which causes floating gates that affect both the p-subcircuit and the n-subcircuit.

The organization of the remaining sections is as follows. Section 2 models the conditions required for stuck-at tests to detect interconnect breaks in a circuit. Section 3 does a worst-case analysis of the detection of these breaks and calculates the minimum length of a test vector required to detect such defects with a specified confidence level, using n-detection principles. Section 4 introduces a statistical model with certain simplifying assumptions, based on

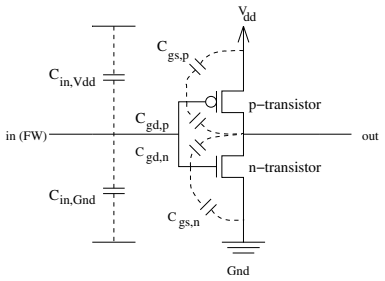

Figure 3: Important capacitances in an Inverter with FW

the length distribution of the wires surrounding the floating wire. We compute the detection probabilities of such breaks using this model and show that the worst case of detection is when the bias voltage is the logic threshold voltage. Section 5 describes and analyses the mathematical model introduced in the previous section, and uses length distribution of surrounding wires to compute the probability of a break. Finally, section 6 summarizes the conclusions that can be drawn from this paper.

2. MODELING BREAKS USING STUCK-AT TESTS

In the following model, we will consider only complete non-resistive breaks. Assuming that we have a CMOS circuit with high quality gate oxide, the input impedance of the gate is very high. The leakage current time constant is also high, generally in the order of hours. Since test application time is in the order of seconds, there will be negligible leakage current during testing. In our model, we are therefore assuming the trapped charge on a floating wire to be constant.

In Figure 2 the trapped charge on the FW ($Q_{trapped}$) equals the charge on the wiring (Q_{wire}) plus the charge on the gates of the transistors that the FW is connected to (Q_{gate}), i.e. $Q_{trapped} = Q_{wire} + Q_{gate}$. Q_{gate} determines the logic value of the output of the gate. Since trapped charge is a constant, if more charge resides in the wiring, then less charge is present on the gate, resulting in a certain logic value at the output. If the charge was distributed in the opposite way, then the logic value on the output could be different. Thus given a value of $Q_{trapped}$, the logic value of the output of a gate with a floating input depends on Q_{wire}.

Q_{wire} depends on the capacitance and voltage on the surrounding wires, which are either at V_{dd} or Gnd in digital circuits. In Figure 3, $C_{in,V_{dd}}$ and $C_{in,Gnd}$ are the total capacitances of the FW to the surrounding signal wires at logic one and logic zero respectively, while $C_{gs,p}$ and $C_{gd,p}$ are the capacitances of the gate to the source and gate to the drain of the p-transistor, respectively. $C_{gs,n}$ and $C_{gd,n}$ are analogous for the n-transistor.

In this analysis, we will make the following assumptions:

1. The interconnect open is assumed to be open-circuit with infinite resistance.

2. In considering the effect of the surrounding wires, we actually consider the capacitive coupling effect due to

only the wires adjacent to the FW. This is a reasonable assumption, considering the fact that wires not adjacent to the floating wire would not have a significant effect compared to the effect due to the adjacent wires, as capacitance falls off quickly with distance and increased shielding.

3. $C_{gs,p}$ and $C_{gd,p}$ are small compared to $C_{in,V_{dd}}$ and $C_{in,Gnd}$. This is because as the sizes of transistor gates are decreasing and interconnect wiring capacitance is increasing, gate capacitances are becoming negligible compared to surrounding wire capacitances. In our model, we have made the simplifying assumption of neglecting $C_{gs,p}$ and $C_{gd,p}$. The same assumptions are made for $C_{gs,n}$ and $C_{gd,n}$.

4. All adjacent wires are equidistant from the FW, as is usually the case with most routers.

5. The threshold voltage V_{TH} is the same for all gates, and is approximately equal to $\frac{V_{DD}}{2}$.

6. The capacitance per unit length of the adjacent wires is constant, based on the assumption that all wires adjacent to the floating wire are equidistant from it. We can say that capacitance is directly proportional to the length. By length of an adjacent wire we mean the length of a wire that is adjacent to the FW.

In this model, we are considering a single logic threshold for the gate output. In general, CMOS circuits are modeled as having two logic thresholds, one for logic zero and the other for logic one. But that is generally due to process variation, which gives different threshold values for different gates in the circuit, so that a consistent model has to have a maximum and a minimum threshold to depict the range of different gate thresholds in the circuit. However, each individual gate has a single threshold and the output of the gate is driven by succeeding gates to a single logic value.

From the above assumptions, if a test results in more surrounding wire lengths at logic zero than at logic one, then $C_{in,Gnd}$ will be greater than $C_{in,V_{dd}}$. This will attract positive charge to the wire (Q_{wire} increases), which pulls charge away from the gates (Q_{gate} decreases) and as a result the p-transistor may be turned on, while the n-transistor may be turned off. This would make the output logic value of the affected gate a logic one. If the test also results in a sensitized path from the gate's output to a primary output, this is a test for the FW sa0. By similar logic, if there are more surrounding wires at logic one and a sensitized path from the gate to a primary output, then it is a test for the FW sa1.

This is true for any fully-complementary *CMOS* gate when the other inputs of the circuit, other than the FW, sensitizes the output of the gate to the value on the FW. This is a necessary condition for all stuck-at tests. [1]

3. DETECTION PROBABILITIES

Let $P(\text{detected}|\text{sa0 test}) = \alpha$ denote the probability of detecting the break by applying a randomly selected sa0 test, $P(\text{detected}|\text{sa1 test}) = \beta$ be the probability of detecting the break by applying a randomly selected sa1 test. So the probability of not detecting the break by applying a randomly selected sa0 test is $P(\text{not detected}|\text{sa0 test}) = 1-\alpha = \alpha'$, and the probability of not detecting the break by applying a randomly selected sa1 test is $P(\text{not detected}|\text{sa1 test}) = 1-\beta = \beta'$.

We assume that the logic values of the wires during one test are independent of the values of the wires during another test. Thus, the distribution of logic values on the wires is independent of whether a sa0 or a sa1 test is applied. With this simplifying assumption, $\alpha+\beta = 1$ (we will shortly discuss the case when this is not true). Then $P(\text{not detected}|\text{sa1 test}) = \beta' = \alpha$ and $P(\text{not detected}|\text{sa0 test}) = \alpha' = \beta$. This is true because the same length of adjacent wires needs to be at a logic 0 for the FW to be at logic 0 so that we can detect the FW as a sa0 fault as cause it to not be detected as a sa1 fault. If a break is not detected by a set of one sa0 and one sa1 test, then the test for the sa0 and the sa1 test must have both failed (i.e. not detected the break). Let the probability of not detecting the break by applying a randomly selected sa0 test and one randomly selected sa1 test be $P(\text{not detect break} \mid 1\text{ sa0} \wedge 1\text{ sa1})$. Assuming that the values on the wires during one test are independent of the values on the wires during another test, and considering $\alpha+\beta = 1$, we get:

$$P(\text{not detect break}|1\text{ sa0} \wedge 1\text{ sa1}) = \beta' \cdot \alpha' = \alpha - \alpha^2$$

This probability is maximum when $P(\text{detected}|\text{sa0 test}) = \frac{1}{2}$. Now, if we apply n sa0 tests and n sa1 tests (n-detection) [7, 10], then the probability of not detecting the break falls off as $(\alpha\beta)^n$. We can explain this as follows. Each of the n sa1 tests has a $P(\text{not detected}|\text{sa1 test}) = \alpha$ and each of the n sa0 tests has a $P(\text{not detected}|\text{sa0 test}) = \beta$. Assuming all tests are independent, the total $P(\text{not detect break } |n \text{ sa0} \wedge n \text{ sa1}) = (\alpha\beta)^n$. Thus, with n sa0 and n sa1 tests, the probability of detecting the break approaches one as n increases. If instead, we apply n sa1 tests and m sa0 tests, then using differential calculus we can say that $P(\text{not detect break} \mid \text{n sa0} \wedge \text{m sa1}) = (\alpha^n\beta^m)$ is maximum for $\alpha = (\frac{n}{n+m})$.

Under certain conditions, the assumption that $\alpha+\beta = 1$ and consequently $\alpha'+\beta' = 1$ might not be true. Due to dependencies between logic values in different wires, $\alpha'+\beta'$ might deviate slightly from 1. We illustrate one situation in which this kind of dependency may arise. Consider Figure 4, where we have the floating wire FW connected to the output of an OR-gate. Without dependencies between wires, that is, without capacitive coupling between adjacent wires, by previous assumption, we have $\beta' = 1-\alpha'$. Let $\alpha' = x$. Therefore, $\beta' = (1-x)$. Now to test the FW with a sa0 test, we will have to put a 1 on one of the input wires i.e on either a or b. The possible input combinations are 10,01,11. Thus we see that $\frac{2}{3}$ of the time, the input wire b will have a 1 on it. If wire b is adjacent to the FW, then there will be capacitive coupling as shown in Figure 4. When b has a 1 on it, then the voltage on the FW will increase $\frac{2}{3}$ of the time. Thus in this case the sa0 test is more likely to fail in detecting the break due to tendency of wire b having a one on it and increasing the voltage on the FW. This implies that $P(FW = 1|\text{sa0 test}) \equiv P(\text{not detected}|\text{sa0 test}) = \alpha'$ increases by an amount say δ, where $0 < \delta < 1$. Therefore, $\alpha' = x+\delta$. Again, to test the FW with a sa1 test, we will have to put a

[1] Note that interconnect opens causing floating gates are different from the *stuck-open*, which is a high-impedance state caused by a faulty pull-up or pull-down transistor network in a CMOS gate [17, 9, 11, 12, 5].

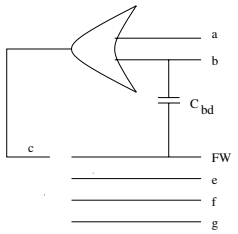

Figure 4: *FW* as output of OR gate, with effective capacitance shown

0 on both the input wires i.e on a and b. Now, when b has a 0 on it, then due to capacitive coupling between adjacent wires, the FW will tend to have a 0 on it [Figure 4]. Thus in this case the sa1 test is more likely to fail in detecting the break which implies that P(not detect¡ed|sa1 test) $= \beta'$ increases by an amount say ϵ, where $0 < \epsilon < 1$. Therefore, $\beta' = (1-x)+\epsilon$. Hence in this case $\alpha' + \beta' = 1 + \delta + \epsilon = k_2$, where $k_2 > 1$. With similar logic we can argue that there are cases in which $\alpha' + \beta' = k_1$, where $k_1 < 1$. Thus, taking dependency into account we can have $\alpha' + \beta' \neq 1$. To solve the problem of finding the worst-case detection probability when $\alpha' + \beta' \neq 1$, we find the maximum value of P(not detect break | 1 sa0 $\wedge$ 1 sa1)$= \alpha'\beta' = z$ (say), subject to the constraint equation $k_1 < (\alpha' + \beta') < k_2$, where $k_1 < 1 < k_2$. It can be shown by straightforward calculation that the optimal solution of this constrained optimization problem is $\alpha' = \beta' = k_2/2$.

Now if d_n^f is the *n-step detection probability* [1] that we detect a break f (at least once) by applying n sa0 and n sa1 tests with P(not detected | sa0 test) $= \alpha'$ and P(not detected | sa1 test) $= \beta'$, then $d_n^f = 1 - (\alpha'\beta')^n$. The detection quality d_n of a test sequence is the lowest n-step detection probability among the stuck-at faults in the circuit. Therefore, $d_n = \min_f\ d_n^f = 1 - [(\alpha'\beta')_{max}]^n$. This formula determines the detection quality of the tests.

To determine the number of sa0 and sa1 tests, n, required to achieve a *level of confidence* of at least c in detecting a break, choose n to satisfy $d_n \geq c$. This is justified because the test length that is long enough to detect the most difficult break with probability c will detect any other break f with $d_n^f \geq c$ [1]. Therefore, $((\alpha'\beta')_{max})^n \leq 1 - c$. This implies that the lowest value of n required to achieve a *confidence level* of at least c in detecting a break is:

$$n_l = \left\lceil \frac{\ln(1-c)}{\ln((\alpha'\beta')_{max})} \right\rceil \quad (1)$$

Now consider F breaks in the circuit under test, with probability of not being detected by a sa0 and a sa1 test equal to $((\alpha'\beta')_{max})$. It can be shown using the above result that the lowest value of n required to achieve a *confidence level* of at least c in detecting *all* the F breaks is:

$$n_{min} = \left\lceil \frac{\ln(1-c^{\frac{1}{F}})}{\ln((\alpha'\beta')_{max})} \right\rceil \quad (2)$$

EXAMPLE 1: If $((\alpha'\beta')_{max}) = 0.5 \times 0.5 = 0.25$ and $c = 0.99$, then, from Equation 1, $n_l = 4$. Thus in this case, when the worst case probability of the break being not detected with a sa0 and a sa1 test is 0.25, we need minimum 4 sa0 and 4 sa1 tests to detect the break with a confidence level of 0.99.

EXAMPLE 2: If there are 100 nodes in the circuit that may have breaks, i.e if $F = 100$ and if the probability of not detecting each of the breaks i.e $((\alpha'\beta')_{max}) = 0.5 \times 0.5 = 0.25$ and $c = 0.99$, then, from Equation 2, $n_{min} = 7$. Thus in this case, when the worst case probability of the most difficult to detect break being not detected with a sa0 and a sa1 test is 0.25, we need minimum 7 sa0 and 7 sa1 tests to detect *each* break in the circuit with a confidence level of 0.99. Note that this is a very pessimistic bound, since in practice α and β values will be in general not equal to the worst-case value of 0.5.

The above examples show that the understanding of the detection of interconnect opens must be refined from the current worst-case analysis to obtain more useful lower bounds on the number of stuck-at tests needed for their detection.

4. ESTIMATION OF PROBABILITIES

To enhance the understanding of the faulty behavior of the circuit, we use the fact that capacitance is proportional to length and construct a length distribution model, using independence of values on the wires. To get an estimate of α and β from our model, we would like to estimate:

$$1.\text{Probability}\left(\frac{C_{in,V_{dd}}}{C_{in,Gnd}} < 1\right), \text{to calculate } \alpha$$

$$2.\text{Probability}\left(\frac{C_{in,V_{dd}}}{C_{in,Gnd}} > 1\right), \text{to calculate } \beta$$

From the assumptions made in this paper, capacitance is directly proportional to the wire length. Thus we can estimate the probability of detecting an interconnect break with stuck-at tests by using the probability distribution of the ratio of total length of surrounding wires at logic one (T_{l1}) to the total length of all surrounding wires (T_l). Such wirelength distributions are available for CMOS circuits [14, 15, 3]. Here we consider a simplified discrete wirelength distribution model for illustrating the concepts.

The voltage on the floating wire without capacitance from the signal wires is important in determining α and β. We call this the bias voltage. How far the bias voltage is from the threshold voltage is a function of the trapped charge on the floating wire, the transistor capacitances and the FW's capacitance to the ground and V_{dd} planes.

We assume the worst case, that the bias voltage is the logic threshold voltage, which means the trapped charge is small [6]. This being the worst case can be easily understood by noting that the presence of trapped charge would either increase P(detected|sa0 test) or P(detected|sa1 test), in either case causing P(not detect break | 1 sa0 $\wedge$ 1 sa1) to move away from the worst case of detection i.e from $\alpha = \beta = 0.5$.

5. ANALYSIS OF THE MODEL

Let there be n signal wires that can affect the charge on the FW. Let each of the n wires have individual lengths. Out of these n wires, let k wires be at logic one. The probability distribution of k is binomial. This is because we assume that the logic value of any of the wires is independent of the other wires' logic values and we can randomly choose a wire from the set of n wires and add it to the set of k wires if it

is at logic one. So this is a series of Bernoulli trials, which gives a binomial distribution.

In order to find the probability $P(T_{l1})$, of k wires at logic 1 adding up to a total length T_{l1}, we see that the total probability of wires at logic one adding up to T_{l1} is

$$\begin{aligned} P(T_{l1}) &= \sum_{i=0}^{n} P(k=i) \cdot P(i \text{ wires add to } T_{l1}) \\ &= \sum_{k=0}^{n} \left[B_k(n,p) \cdot P\left(\sum_{i=1}^{k} l_i = T_{l1} \right) \right], \end{aligned}$$

where l_i is the length of the i^{th} wire, $B_k(n,p) = \frac{n!}{k!(n-k)!} p^k (1-p)^{n-k}$, and p equals the probability that a wire chosen at random from n wires is at logic 1. Now, taking discrete convolutions,

$$P\left(\sum_{i=1}^{k} l_i = T_{l1} \right) = \sum_{a_1=l_{min}}^{l_{max}} \cdots \sum_{a_{k-1}=l_{min}}^{l_{max}} P(l_1 = a_1) \ldots \ldots P(l_{k-1} = a_{k-1}) \cdot P(l_k = T_{l1} - a_1 - \ldots - a_{k-1}) \quad (3)$$

where l_{min} is the smallest possible length of a wire and l_{max} is the largest possible length of an interconnect wire. Note that the probability values and parameters like l_{min} and l_{max} in the above equation are available from the wirelength estimates [15]. We can also similarly find the distribution of total lengths of wires at logic zero (T_{l0}). To get an idea about the distribution of the total lengths of all surrounding wires (T_l) we use the fact that $l_1 + l_2 + \ldots + l_n = T_l$ to get:

$$P\left(\sum_{i=1}^{n} l_i = T_l \right) = \sum_{a_1=l_{min}}^{l_{max}} \cdots \sum_{a_{n-1}=l_{min}}^{l_{max}} P(l_1 = a_1) \ldots \ldots P(l_{n-1} = a_{n-1}) \cdot P(l_n = T_l - a_1 - \ldots - a_{n-1})$$

This gives us an idea about the total lengths possible, though it does not tell us anything about the actual total lengths permitted given specific values for T_{l1}. Because of this we need to derive the probability of the ratio (T_{l1}/T_l), where $(T_{l1} \leq T_l)$.

5.1 Derivation of Probability of Length Ratio

To arrive at the probability distribution for (T_{l1}/T_l), where $(T_{l1} \leq T_l)$, we calculate the probability for $(T_{l1}/T_l) = \lambda$ as follows:

We see that we can have certain cases, where there are no wires at logic one, that is, all wires are at logic zero. Hence, we have two cases for λ.

Case 1 ($\lambda = 0$): When $\lambda = 0$, we have to calculate the probability of $T_{l1} = 0$ for all values of T_l. For this degenerate case, the resulting probability is:

$$P\left(\frac{T_{l1}}{T_l} = \lambda \right) = P(T_{l1} = 0)$$

Case 2 ($\lambda \neq 0$): When $\lambda \neq 0$, we calculate the probability for each value of $T_{l1} = m$ ($l_{min} \leq m \leq n l_{max}$) and the corresponding value for $T_l = \frac{1}{\lambda} m$, given $T_l \geq T_{l1}$ i.e. $\lambda \leq 1$;

Using the chain rule of conditional probability and Bayes' Theorem [13], it can be shown that:

$$P\left(\frac{T_{l1}}{T_l} = \lambda \right) = \sum_{m=l_{min}}^{n l_{max}} \frac{P(T_{l1} = m, T_{l0} = (1/\lambda - 1)m)}{P(\lambda \leq 1)} \quad (4)$$

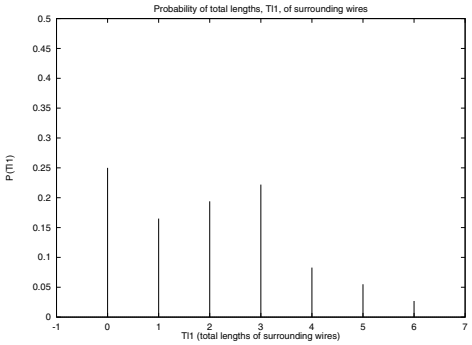

Figure 5: Probability distribution for T_{l1} from Equation 5.

Now, to find $P(T_{l1} = m, T_{l0} = (1/\lambda - 1)m)$, we see that this is the joint probability distribution for T_{l1} and T_{l0}. We look at the problem this way: out of n wires, for k wires to be at logic one, the probability is $B_k(n,p)$ (as explained Section 5). Now the lengths of the k wires have to add up to m, while the lengths of the $(n-k)$ wires have to add up to $(1/\lambda - 1)m$. Without loss of generality, let us take the k wires out of n that are at logic 1 and index them from 1 to k. Also the $(n-k)$ wires that are at logic 0, are indexed from $(k+1)$ to n. Therefore, the numerator in Eqn. 4 is:

$$P(T_{l1} = m, T_{l0} = (1/\lambda - 1)m) = \sum_{k=1}^{n} [P(\sum_{i=1}^{k} l_i = m) \cdot P(\sum_{i=k+1}^{n} l_i = (1/\lambda - 1)m) \cdot B_k(n,p)] \quad (5)$$

Using the discrete convolution calculation of Equation 3 in Equation 5, we can finally compute the value of $P\left(\frac{T_{l1}}{T_l} = \lambda \right)$ from Equation 4. Note that in this derivation we have considered the length distribution to be discrete and hence we have performed discrete convolutions. If the length distribution is continuous, then we do continuous convolutions.

5.2 Example

Let us compute the total probability distribution for the ratio (T_{l1}/T_l) in the following example. Let there be two wires ($n = 2$) with possible lengths of one, two and three, with probability of occurring of $\frac{1}{3}$, $\frac{1}{3}$, and $\frac{1}{3}$, respectively.

For this case, if we compute the distribution for T_{l1}, using Equations 3 and 5 in Section 5, we would get the graph in Figure 5.

The probability distribution for the ratio of (T_{l1}/T_l) is shown in Figure 6. From Figure 6, we see that $P(\lambda = 0) = 0.25 = P(\lambda = 1)$ is greater than all other $P(\lambda)$ values, as expected.

When we plot the curve of $P(\lambda)$ vs. λ, the sum of the probabilities of (T_{l1}/T_l), when $\lambda > 1/2$, equals P(detected|sa1 test). The sum of the probabilities of (T_{l1}/T_l), when $\lambda < 1/2$, equals P(detected|sa0 test).

From Figure 6, we see that $P(\lambda) = \frac{1}{6}$ for $\lambda = \frac{1}{2}$. Now, due to noise in the circuit, we can say that half of the time, $\lambda = \frac{1}{2}$ will contribute to P(detected|sa1 test), while half of the time, $\lambda = \frac{1}{2}$ will contribute to P(detected|sa0 test). Hence in the case of this example we can say that

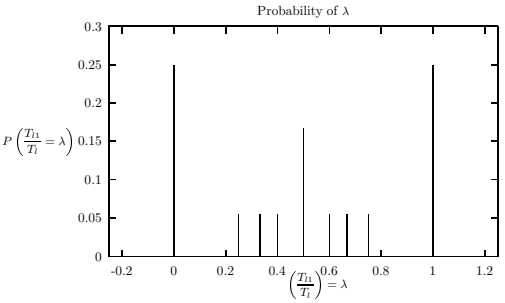

Figure 6: Probability distribution for example in Section 5.2.

λ	$P(\frac{T_{l1}}{T_l} = \lambda)$
0	1/4
1/4	1/18
1/3	1/18
2/5	1/18
1/2	1/6
3/5	1/18
2/3	1/18
3/4	1/18
1	1/4
$\sum P(\frac{T_{l1}}{T_l} = \lambda) = 1$	

Table 1: Table showing the permitted values for λ and their associated probabilities.

$P(\text{detected}|\text{sa0 test}) = \alpha = \frac{1}{4} + \frac{1}{18} + \frac{1}{18} + \frac{1}{18} + \frac{1}{2} \times \frac{1}{6} = 0.5$. Thus, $P(\text{detected}|\text{sa1 test}) = \beta = 0.5$ also. Now, we showed earlier that when the logic values on the surrounding wires during one test are independent of the logic values on the wires during another test, i.e when $\alpha = (1 - \beta)$, as in the case of this model, then we have the worst case of detection when $\alpha = \beta = 0.5$. The primary assumption in this model was that the bias voltage is the logic threshold voltage and from that the model gives us the worst case of detection.

6. SUMMARY AND CONCLUSIONS

This paper provides an initial framework for the investigation of detecting interconnect break defects. We first modeled the conditions required for a stuck-at test to detect interconnect breaks in a circuit and presented an argument showing that it is likely that floating nodes' voltages would be close to the logic threshold of the circuit, which is the worst case condition for detection by logic tests. We then presented an analysis of the probability of detecting a fault taking into consideration both independence and dependence of the logic values on the wires. Using n-detection principles, we calculated the minimum number of test vectors required to detect all breaks in the circuit with a specified confidence level, given worst-case values for α and β.

Using the worst case assumptions, the number of times a node must be tested to guarantee detection of all breaks in the circuit with a high confidence level is quite high. Since ICs are considerably more reliable than the predicted given worst-case values for α and β, in most cases we will not meet the worst case conditions.

To enhance the understanding of the faulty behavior of the circuit, we constructed a detailed probabilistic model based on the length distribution of the wires surrounding the floating wire. With certain simplifying assumptions, we used this model to compute the detection probabilities of the break using stuck-at-0 and stuck-at-1 tests. From this model we showed that we have the worst case of detection when the bias voltage is the logic threshold voltage.

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