Multi-peak Bandwidth Enhancement Technique for Multistage Amplifiers

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ABSTRACT
A new technique for designing wideband multistage amplifiers (MA) is introduced. The proposed method has several advantages such as increased bandwidth with increasing number of stages and decreased sensitivity to process variations. All stages of the proposed MA topology can be identical, where the bandwidth can be several times more than that of a single stage. A 0.35μm CMOS process is used to implement the new MA circuit; where active negative feedbacks exploit the intrinsic capacitance within the transistors to expand the bandwidth. Simulation results show an overall GBP of 4.8THz.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]

General Terms
Design

Keywords
Wideband Amplifier, Multistage Amplifier, Peaking Technique, Optical Communications

1. INTRODUCTION

High-speed multistage amplifiers (MA) are widely used in optical communications systems as the main amplifier in a receiver. Multi-stage amplifiers must have high gain and wide bandwidth with frequency response from DC range to several GHz to provide the following Clock and Data Recovery (CDR) circuit with uniform output level regardless of input swing level. Also, low phase shift deviation and crossing point fluctuation must be insured over a wide input dynamic range to avoid degrading the sensitivity and phase margin of CDR [1].

Figure 1 shows an *n*-stage conventional MA, which consists of *n* gain stages $g_1(s)$,…, $g_n(s)$. Assuming that all stages have the same

GLSVLSI'04, April 26–28, 2004, Boston, MA, USA.

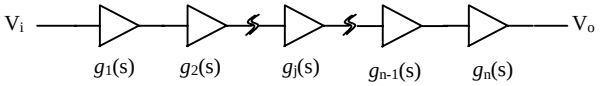

Figure 1. *n*-stage conventional MA

single dominant pole ($\omega_{p1}=\omega_{p2}=\ldots=\omega_{pn}=\omega_p$) and the same DC gain of *G* as

$$g_j(s)=\frac{\omega_p G}{s+\omega_p} \tag{1}$$

then the overall DC gain and the bandwidth of an *n*-stage MA are obtained by

$$G_T = G^n \qquad \omega_{bw} \approx \omega_p \sqrt{2^{1/n}-1} \tag{2}$$

Expanding the bandwidth of one stage, which is usually placed at the output node of each stage, ω_p, is one of the methods used to broaden the overall bandwidth of an MA [2]-[5]. Some well-known bandwidth enhancement methods are: using peaking capacitors, capacitance neutralization and shunt-peaking. Peaking techniques enhance ω_p by introducing a peak in a transfer function at high frequencies. However, increasing ω_p is not enough for bandwidth enhancement since the combination of the poles of all stages degrades the overall bandwidth, ω_{bw}. For a conventional MA ω_{bw} is always less than ω_p when $n>1$.

To further increase the overall bandwidth of a conventional MA of Fig. 1, stages can be designed to have different gains and poles to introduce peaks at different frequencies. This approach was used to design a transimpedance amplifier [6], where an early roll-off due to a low frequency pole in one stage was compensated with peaking in the next stage. There are two drawbacks in using this multi-pole enhancement. First, the design of stages is not uniform and each stage should be designed separately. Second, process variation may result in an undesirable peaking. Sensitivity of stages with high quality factor limits the usage of these circuits in typical applications (sensitivity is related to 2Q).

This paper introduces the chained multistage amplifier (CMA), which utilizes a new technique to expand the bandwidth of an MA by applying a chain of active feedbacks. The proposed circuit topology exploits the intrinsic capacitance within the transistors to push output pole of each stage to a higher frequency. CMA offers several advantages such as improved performance and gain-

bandwidth product that make it suitable for optical communications applications. To validate the proposed topology, several MAs in 0.35μm CMOS process were designed and simulated. In section II, the CMA topology and its features are discussed. The circuit implementation is described in Section III. Simulation results are presented in Section IV. Finally, summary of the results is given.

2. CHAINED MULTISTAGE AMPLIFIER

Active feedback enhances the bandwidth by using the peaking technique. Figure 2 shows the block diagram of the proposed structure, n-stage chained multistage amplifier (CMA). Assume that the amplifier blocks $g_i(s)$ can be represented as in Eq. (1) and the feedback blocks have the transfer function

$$f_j(s) = \frac{\omega_p F}{s+\omega_p} \tag{3}$$

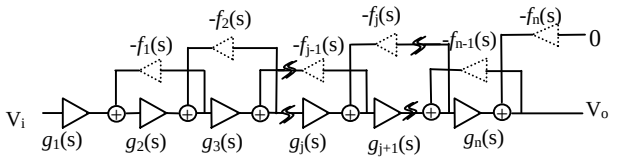

Figure 2. CMA topology

Let us consider the case of n=2. The two-stage topology has a second-order transfer function with the natural frequency, quality factor and 3dB bandwidth given as

$$\omega_n = \omega_p\sqrt{1+GF} \qquad Q = 0.5\sqrt{1+GF} \tag{4}$$

$$\omega_{bw} = \omega_p\left[GF - 1 + \sqrt{2\left[(GF)^2+1\right]}\right]^{0.5} \tag{5}$$

For Q>0.707 (or GF>1) the bandwidth can be improved up to $2.7\omega_p$, while the maximum peak on the overall DC gain is less than 1.5dB ($@GF \le 3.34$). To better understand the bandwidth enhancement technique of CMA, consider the case of n=4 where the 4th-order transfer function can be presented as a product of two 2nd-order transfer functions with ω_{n1}, ω_{n2}, Q_1 and Q_2 of

$$\omega_{n1} = \omega_p\sqrt{1+0.38GF} \qquad \omega_{n2} = \omega_p\sqrt{1+2.62GF} \tag{6}$$

$$Q_1 = 0.5\sqrt{1+0.38GF} \qquad Q_2 = 0.5\sqrt{1+2.62GF} \tag{7}$$

Since ω_ns and Qs are different, each 2nd-order transfer function has a peak at a different frequency. The overall bandwidth of 4-stage CMA can be improved up to about $2.9\omega_p$ without incurring a significant peak (<1.5dB) in its transfer function. Similarly, the overall bandwidth can be increased several times more than ω_p for n=6 and 8, and it can be approximated by

$$\omega_{bw} \approx (1+GF)\omega_p\sqrt{2^{1/n}-1} \quad , \quad n=2,4,\ldots,8 \tag{8}$$

Equations 2 and 8 show that the CMA has a bandwidth of (1+GF) times that of a conventional MA.

The total gain-bandwidth product (GBP) of the CMA is less than that of the conventional MA. Another parameter that shows performance of an MA is the gain-bandwidth product of one single stage, GBP_1, which is given as [7]

$$GBP_1 = (Overall\ \ Gain)^{\frac{1}{n}} \times (3-dB\ bandwidth) \tag{9}$$

GBP_1 of the conventional MA is decreased as n increases whereas GBP_1 of the CMA can be increased as n increases. This is confirmed by the circuit simulation results (see Section IV).

The advantages of the proposed CMA topology can be summarized as follows:

- The bandwidth can be several times more than ω_p; whereas for n-stage conventional MA ω_{bw} is always less than ω_p (see Eq. (2)).
- CMA can have more bandwidth as n increases. As shown above, 4-stage CMA can be broader than 2-stage CMA; on the contrary, 4-stage conventional MA has less bandwidth than 2-stage conventional MA (see Eq. (2)).
- CMA does not require stages with high quality factor, which are very sensitive to process.
- All amplifier stages of the CMA can be identical.
- The GBP_1 can be increased as n increases.

3. CIRCUIT IMPLEMENTATION

The amplifier stages in Fig. 2 were implemented using an inductorless differential cascode structure with gain boosting as shown in Fig. 3. A six-stage CMA, which was implemented in this paper, is illustrated in Fig. 4.

Using cascode structure decreases the effective input capacitance of individual stages and increases the forward gain. Gain boosting shifts the pole of the M_g's drain node (see Fig. 3) to higher frequencies. Adding a new pole to the gate of M_L is a drawback of using gain boosting. To ensure high-frequency operation, the gain of booster should be small. In the model used, the poles associated with the source node and the gate node of the transistor M_L is considered far from the dominant pole, which is placed at the output node of each stage.

The overall output capacitance of each stage is reduced by using the Miller effect of C_{gd} of transistor M_f in Fig. 3. Consider the simplified circuitry of a two-stage CMA as illustrated in Fig. 5. The second stage is a simple DC amplifier with the gain block G and the input capacitor C_i, whereas the first stage is modeled using a voltage-controlled current source ($g_{mg}V_i$), a load resistance (R_L) and the output capacitor (C_o). The voltage-controlled current source $g_{mf}V_o$ represents the feedback from the second stage. The node X has the overall capacitance of $C_{eq} \cong [C_o + C_i + C_{gdf}] - GC_{gdf}$. C_{eq} can be reduced by increasing G and C_{gdf}. However, G cannot be increased to an arbitrarily large value for a constant R_L, since it increases C_i. Furthermore, increasing C_{gdf} decreases the overall gain. Therefore, there is a trade-off between the overall gain and bandwidth.

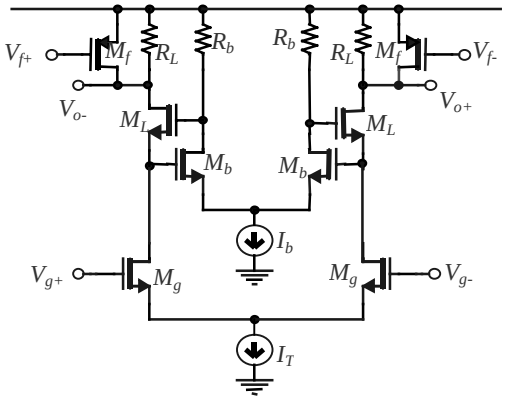

Figure 3. Cascode amplifier used in CMA

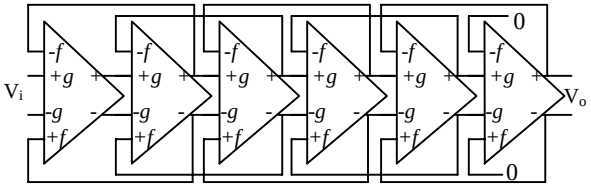

Figure 4. Implementation of a 6-stage CMA

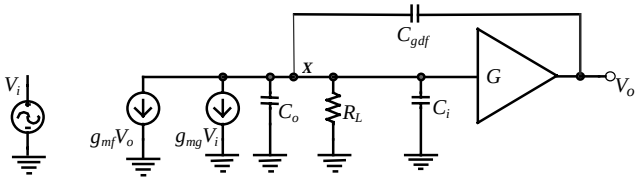

Figure 5. Simplified circuit of a two-stage CMA

Using extra transistors M_f in Fig. 3 does not increase power consumption significantly, since the drain current of M_f is much less than that of M_g ($I_g >> I_f$).

4. SIMULATION RESULTS

Several CMAs and conventional MAs were designed for *n=2, 4, 6 and 8* using 0.35μm CMOS technology. The amplifiers were optimized with different W_f (width of the transistor M_f) and R_L to have the minimum ripple (<1.5dB) in their transfer function, where the forward DC gain (G) was kept constant for all stages (MAs' stages do not have M_f). The circuits were combined with a buffer to drive the 50Ω loads in series with 1pF capacitors at 3.3V single power supply. Figure 6 illustrates the simulation of AC responses (@ $GF \approx 1$). The CMA has a wider bandwidth and the simple cascade structure without feedback gives a larger gain. 8-stage CMA has a bandwidth of about 2.9 GHz and a DC gain of about 60dB, while 8-stage MA has a bandwidth of about 0.43 GHz and a DC gain of 91dB.

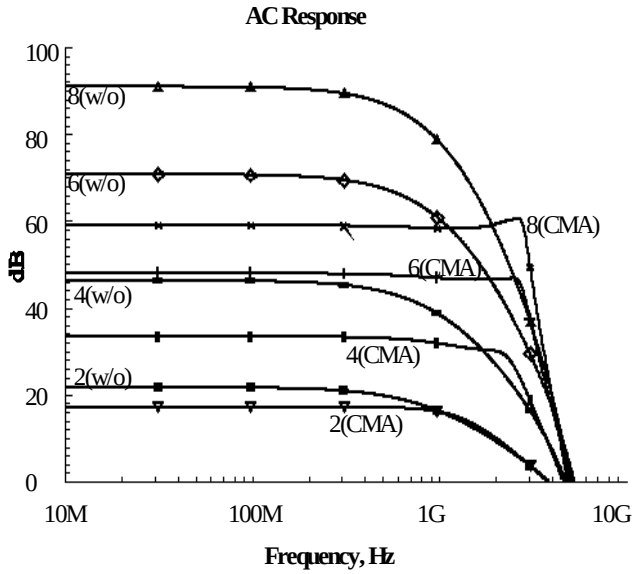

Figure 6. AC Response Simulation of the gain of the CMAs and the conventional MAs (w/o) for n=2, 4, 6 and 8

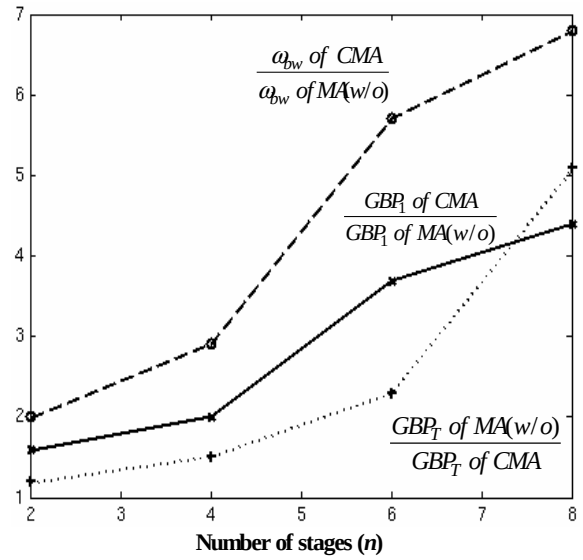

Figure 7. Ratio of Bandwidth and GBP_1 of *n*–stage CMA and *n*-stage conventional MA (w/o) *and* Ratio of Total Gain Bandwidth Product (GBP_T) of *n*-stage conventional MA (w/o) and an *n*-stage CMA

To compare the CMAs and MAs for *n=2, 4, 6 and 8*, their GBP_1s and the overall GBPs (GBP_T) were calculated from simulations. GBP_1 of CMA for *n=2, 4, 6 and 8* are 3.70GHz, 4.21GHz, 6.88GHz and 7.38GHz, respectively. The ratio of GBP_1s and the bandwidths for two structures of CMA and MA is illustrated in Figure 7. The CMA's GBP_1 is higher and increasing *n* gives a higher GBP_1 for CMA. This is exactly the opposite of what is seen in the conventional MA. As Fig. 7 shows, the bandwidth of CMA is more than 6.8 times of that of the MA. As it was explained, the topology of CMA expands the overall bandwidth with (1+*GF*), e.g., for *GF=1*, it doubles the bandwidth. The Miller effect of C_{gdf} shifts the dominant pole of stages (1 to *n*-1) to

higher frequencies by up to four times. Dominant pole of the last stage is different from others. Having more stages introduces more peaks and compensates for rolling-off of transfer function affected by the dominant pole of the last stage. Figure 7 also illustrates the ratio of the overall gain-bandwidth product (GBP_T) of the MA and the CMA. As it shows, this ratio is increasing as *n* increases. Compared bandwidth ratio, it is lower.

Figure 8 illustrate group delays of CMAs and MAs. Unfortunately, the group delay of the CMA has a peak around the corner frequency, and its variation increases as *n* increases (the same behavior can also be observed for a conventional MA). This can be predicted because having separated poles causes more variation in group delay. For n=8 and 10^4 random bits with the rate of 2.5Gb/s, eye diagrams of CMA and MA for an input signal of 1V peak-to-peak are shown in Figs. 9 (a) and (b). Figures 9 (c) and (d) show the eye diagrams for an input signal of 1mV peak-to-peak. The power consumption of each stage is less than 9mW. Input referred noise of CMA is $2(nV/(Hz)^{0.5})$-$3(nV/(Hz)^{0.5})$. Noise of the conventional MA is $1(nV/(Hz)^{0.5})$-$2(nV/(Hz)^{0.5})$.

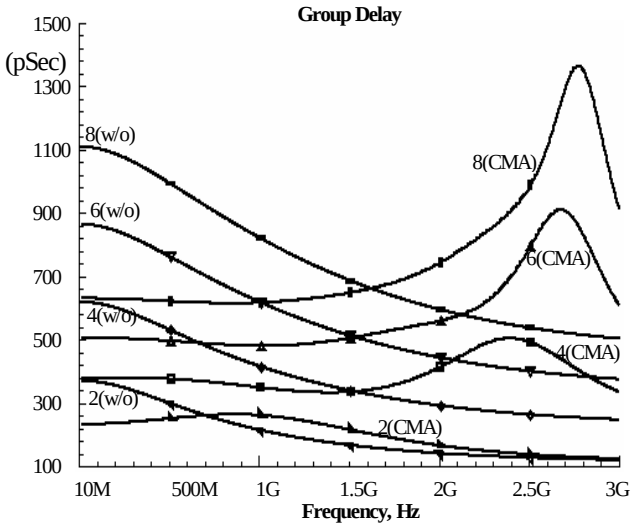

Figure 8. Group Delay simulation result of *n*–stage conventional MA (w/o) and *n*-stage CMA for *n*=2, 4, 6 and 8

5. CONCLUSION

A new technique for designing a wideband multistage amplifier was introduced. The proposed method, chained multistage amplifier (CMA), uses active feedback to improve the bandwidth. Due to lower quality factor required, CMA has lower sensitivity to process variations. Furthermore, identical gain stages can be used to build the CMA, which simplifies the design process. An 8-stage CMA was designed in 0.35µm CMOS process, where more than 2.9GHz bandwidth and an overall GBP of 4.8THz were obtained from simulations.

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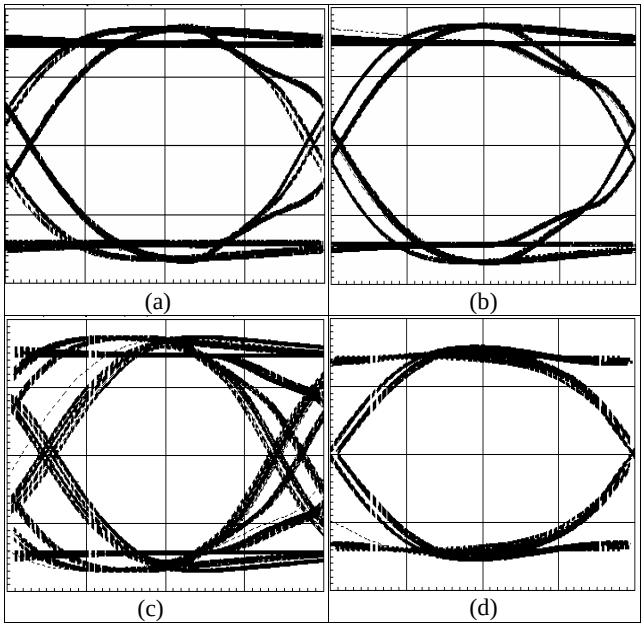

Figure 9. Eye diagrams for an input signal of 1V peak-to-peak (a) MA, (b) CMA and of 1mV peak-to-peak (c) MA and (d) CMA (Div X=100pSec and Div Y=200mV)