PANEL

Nanometer Design: Place Your Bets

Chair: Andrew B. Kahng, University of California at San Diego

Organizers: Gloria Nichols & Bing Sheu

Panelists: Shekhar Borkar, Intel, John Cohn, IBM, Antun Domic, Synopsys, Patrick Groeneveld, Magma, Louis Scheffer, Cadence, Jean-Pierre Schoellkopf, STMicroelectronics

Overview

Two years ago, DAC-2001 attendees enjoyed a thrilling debate-panel, "Who's Got Nanometer Design Under Control?", pitting sky-is-falling Physics die-hards against not-to-worry Methodology gurus. Then, the DAC audience overwhelmingly voted the match for the Methodologists. Now, we've just gone through the biggest business downturn in the industry's history, and we're hearing more and more about chip failures due to 130nm physical effects. Both physics and economics are a lot worse than we thought two years ago. Where are those simple, correct-by-construction methodologies for signal integrity, power integrity, low-power, etc. that we were promised? Were we bamboozled by glib promises from those Methodologists?

In this session, we bring back the panelists from two years ago, not for another debate, but to hear well-reasoned perspectives on how to prioritize spending to address nanometer design challenges. Yes, methodology can solve any problem – but now we want to know which problems, in what priority order, at what cost. The panel will address the following questions.

- What are the economic impacts and significance of the key nanometer design challenges, *relative to each other*?
- Which nanometer design problems merit responsible R&D investment, in what amounts and proportion?
- What is the likelihood of success, both near-term and long-term, in solving key nanometer design challenges?
- Where will the answers come from?

To keep the discussion very concrete, each panelist will be given a $100 budget, and must defend their allocation of this budget to attack various design problems. Where should the $100 be spent? The audience will determine the best-reasoned allocation, and the winning panelist keeps all the money.

Panelist Statements

Shekhar Y. Borkar, *Intel*

Technology scaling will continue, improving transistor performance, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation, to deliver even more value at a lower cost. The scaling, however, will come with some adverse effects posing perceived barriers. In the 130nm generation and below, subthreshold and gate leakages escalated, and various leakage powers became substantial. As we scale further, parameter variations will become even more prominent, resulting in large variability in performance and power. On the economic front, fab capital expense will probably continue to rise, and the cost of a mask set will increase dramatically. In spite of these technical and economic challenges, which will not be easy, the scaling treadmill will continue well into deep nanometer-scale designs for the compelling reason that it benefits the end user with higher value at a lower cost. It's time for the naysayers, who have been wrong for the last 30 years, to stop whining and get back to work.

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John Cohn, *IBM Microelectronics*

Like everyone else in my business, I have had my share of sleepless nights thinking about performance scaling, signal integrity, reliability, skyrocketing design costs, etc. But rather than spread my money too thin, I want to concentrate on just two problems. Given $100, I'd put the bulk of it, say $65, on process variability and the remaining $30 on power.

The $30 on power is easy. Everyone knows that power is a huge issue, but it's so 2002! The good news on power is that everyone 'gets it', and lots of folks are working on it. The bad news is that we're still having problems predicting power accurately at the gate level, to say nothing of our ability to predict it earlier in the design flow. Beyond analysis, I'd like to see much more work going into power optimization of multi-voltage and multi-threshold design styles. I'd also like to see us get a better handle on power prediction for power supply integrity prediction. I see my $30 to power as helping keep momentum on work that's well underway.

Variability is a completely different story. The more we learn about 90nm and below the more we are beginning to appreciate the range of problems that increasing process variability poses. Variability is forcing us to leave a tremendous amount of performance on the table through excessive over-design. It's costing us leakage power through device length variations. It costs us productivity through increased process corner characterizations, and it's costing us bags of money on yield. I see the biggest challenge here to be reworking our analysis tools to correctly model statistical variations. I predict that the team that gets the first viable design flow based on statistical timing is going to have a huge advantage in the industry. There are also tons that can be done on the control side to manage variability. New RET techniques should be able to reduce the amount of lithography induced variation. New techniques to increase circuit and layout regularity could also be a big help. A better handle on variability will also open up huge opportunities in design centering, speed binning and other yield improvement techniques.

With so many exciting things that we could be doing to address the problem of variability, it's odd that so little serious work in the industry is targeted to solve it. That's why I'm putting my $65 on the odds that folks wake up and see the opportunity. The remaining $5 I'll use to buy lottery tickets…just to hedge my bet.

Antun Domic, *Synopsys*

What problems need to be addressed, and by how much?

The key problem emerging now is coherence of approach along the design process. We continue to measure based on very different criteria at each stage in the design flow, obviously, as further data becomes available. But given the complexity of the new physical phenomena, sharp definitions and understanding of what has been done and how it is measured will be critical to success in matching silicon. A good example is "Signal Integrity": what has really been modeled and extracted, which data has been put into libraries, and how each tool interprets the data will be the keys to success. Note that this is a global problem, and will quickly subsume the current "data transfer" issues being addressed by flows, databases, etc. Without common views on these issues, commercial EDA tools will fail to solve many of the nanometer problems.

Data capacity is another very serious issue needing investment, especially if we consider the "post-tapeout" operations such as OPC, PSM, and fracturing to produce masks (impacting their cost dramatically). The sheer amount of data being handled will require significantly better links to design intent so as to minimize this problem.

Patrick Groeneveld, *Eindhoven Univ. of Technology*

Over the past decades, mask rules have gradually gotten more complicated. Incremental improvements and 'clever tricks' have always enabled conventional place and route algorithms to deal with mask design rules. The new nanometer rules (including process variability and density rules) will be no exception. A short-term investment is required to specify mask design rules in terms of objectives, instead of as a set of hard constraints. In this way, manufacturability can be improved without significantly affecting routability. This requires a more active cooperation between EDA companies and silicon foundries.

Intricate nanometer electrical effects must be dealt with at several steps throughout the flow. The latest generation of EDA tools already have embedded power integrity and crosstalk analysis. It will become infeasible to fix huge numbers of such violations in post-processing steps through analysis and repair. More investments are required to create new design flows that attempt to avoid nanometer issues early on in the design flow.

Although each of the nanometer design issues is solvable, it will most likely require additional silicon real estate and design effort (and with that, cost). The EDA industry must invest in minimizing this cost by a complete automation of each and every nanometer rule. The scale of the circuit simply will not permit human intervention for every nanometer issue.

Louis Scheffer, *Cadence*

From the viewpoint of fundamental physics, there appear to be no showstoppers for the next few nanometer generations. However, there is a horde of practical problems, each of which can (at least potentially) be addressed through process changes, new and improved tools, and/or design methodologies. Here's my personal assessment, in order of criticality (subject to change, of course). Lithography is of course crucial and will get a one-generation boost through OPC, PSM, etc, but after that it's up to the process folks. Leakage control is next in importance and must be addressed by the process people – design techniques are approaching their limits already. Logical correctness must be handled through methodology since there are no new tools in the pipeline. Testing will require some new techniques, else chips will cost more to test than to make, but new tools can help here. Yield improvement and DFM in general, reliability verification, extraction (including inductance), delay calculation, timing analysis, IR drop, package design and analysis, and mask (NRE) costs are all serious problems, but we can muddle through. Of this set, handling process variability is a notch above the others in importance.

Jean-Pierre Schoellkopf, *STMicroelectronics*

Design and verification of complex integrated circuits is becoming sensitive to several new physical effects that have been ignored or minimized or easily handled until now. Power distribution problems have been solved mainly by over-design techniques. Decreasing power supply voltage, while increasing both frequency and circuit complexity, makes basic gates more sensitive to noise on power lines; in the mean time, noise levels are increasing due to increasing current levels amplified by inductive effects (which have been ignored until now). Verification tools are not yet able to handle high-complexity designs: too many RLC components, and it is difficult to take actual timing information into account. Recommended research guidelines are: (0) obviously minimize power consumption at system and design levels, and reduce peak currents, by either asynchronous design or delaying clock events; (1) use a hierarchical approach to model power consumption, following a divide-and-conquer policy as in timing analysis, and being able to characterize current waveforms on power pins as a function of time and input signals; (3) integrate decoupling capacitances using integrated MIM (Metal Insulator Metal) capacitors, which requires good modeling practices and tools to balance internal and external decoupling ; (4) develop efficient RLC extraction tools capable of handling huge complexity and making efficient and accurate reductions ; (5) enforce electromigration rule compliance with tools able to compute maximum current density in every via and metal line; and (6) prefer static and formal verification approaches to dynamic ones, when applicable.