Evolvable Hardware
and its industrial applications

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Contents of this talk

- Basic Concept of Evolvable Hardware

- Digital Hardware Evolution
  - Gate-level Evolvable Hardware
    - EMG prosthetic hand
    - Clock-timing adjustment (Post-fablication adjustment)
    - Data compression for print image data
  - Function-level Evolvable Hardware
    - Autonomously reconfigurable neural network chip

- Analogue Hardware Evolution
  - Analogue EHW chip for cellular phones

- Mechanical Hardware Evolution
  - Evolvable Femto-second Laser System
  - Evolvable Interferometer
  - Evolutionary fiber alignment

EvolvableHardware =

Evolutionary Computation
+
Reconfigurable Hardware

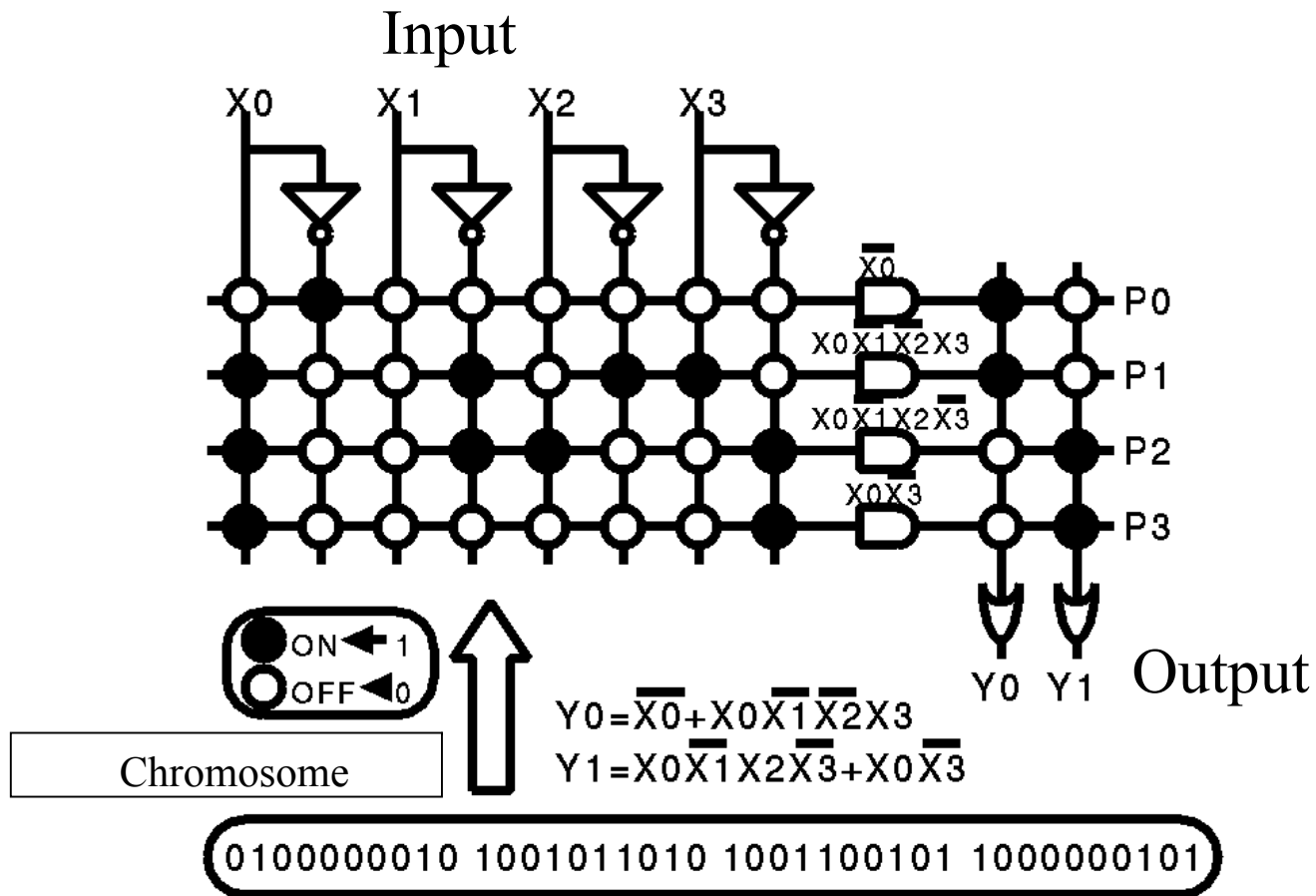# Evolvable Hardware (EHW)

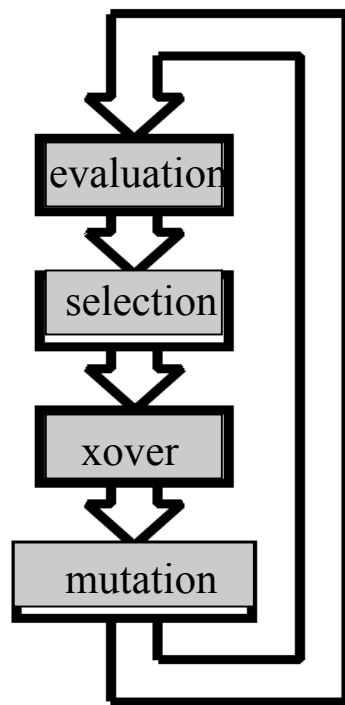| Conventional Hardware	Evolvable Hardware
Specification fixed	Spec. changes dynamically
Architecture fixed	Architecture changeable => Hardware circuit is autonomouly synthesized.

PLA (Programmable Logic Array)

Input

X0 X1 X2 X3

$\overline{X0}$

X0 X1 X2 X3

X0 X1 X2 $\overline{X3}$

X0 X3

P0
P1
P2
P3

● ON ◄ 1
○ OFF ◄ 0

Chromosome

$Y0 = \overline{X0} + X0\overline{X1}\,\overline{X2}\,X3$

$Y1 = X0\overline{X1}X2\overline{X3} + X0\overline{X3}$

Y0 Y1   Output

0100000010 1001011010 1001100101 1000000101

GA (Genetic Algorithm)

Bio-inspired robust search and adaptation
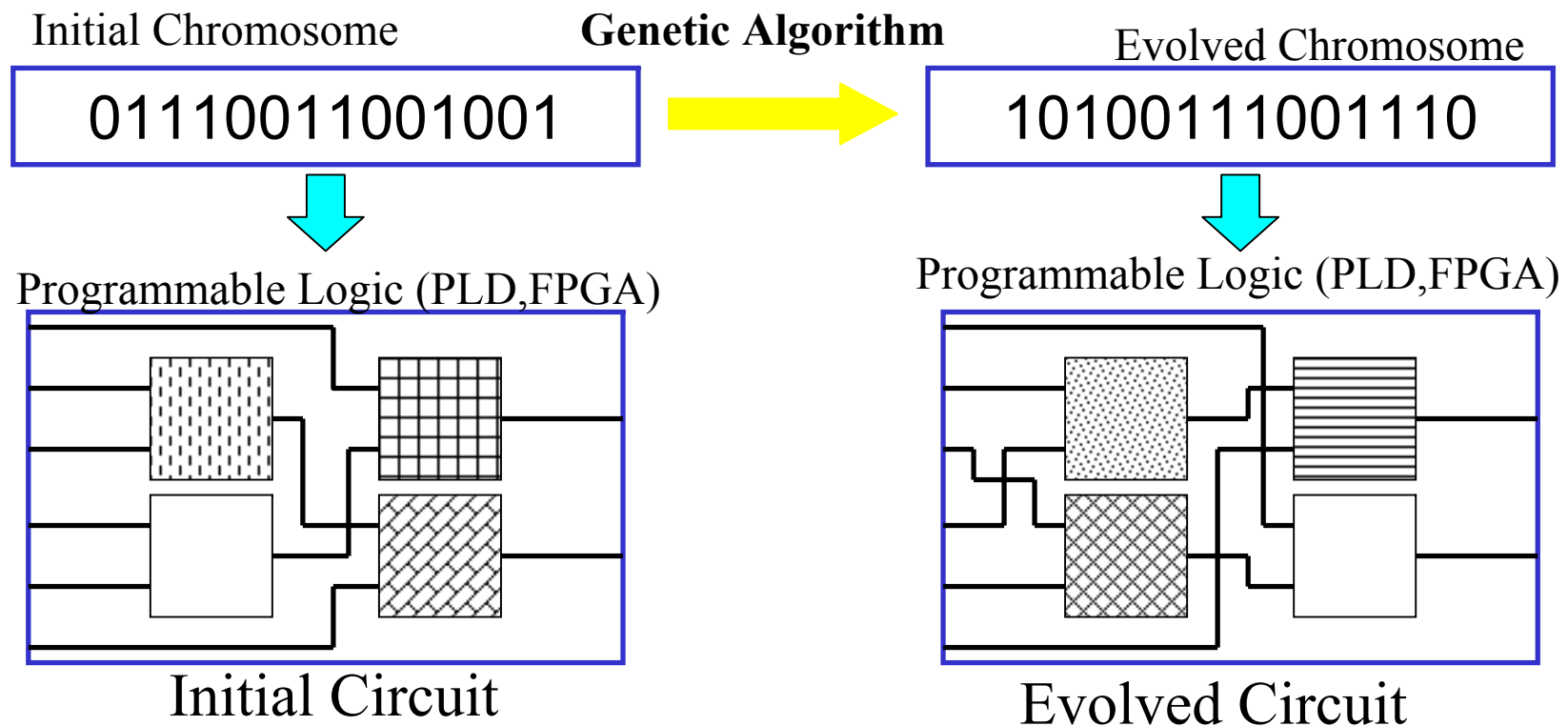
- Selection
  - select high-fitness chromosomes
- Crossover
  - exchange of chromsomes
- Mutation
  - change of chromsomes

evaluation

selection

xover

mutation

Basic idea of Evolvable Hardware

- EHW= Genetic Algorithms + Programmable Logic

Initial Chromosome

01110011001001

Genetic Algorithm

Evolved Chromosome

10100111001110

Programmable Logic (PLD,FPGA)

Programmable Logic (PLD,FPGA)

Initial Circuit

Evolved Circuit

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  - Evolvable Interferometer
  - Evolutionary fiber alignment

Digital Hardware Evolution

- Chromosome determines:
  - types of hardware components
  - interconnections among hardware components
- Gate-level hardware evolution
  - Hardware components are primitive gates such as AND-gate and OR-gate.
- Function-level hardware evolution
  - Hardware components are higher hardware functions such as adders and multipliers.
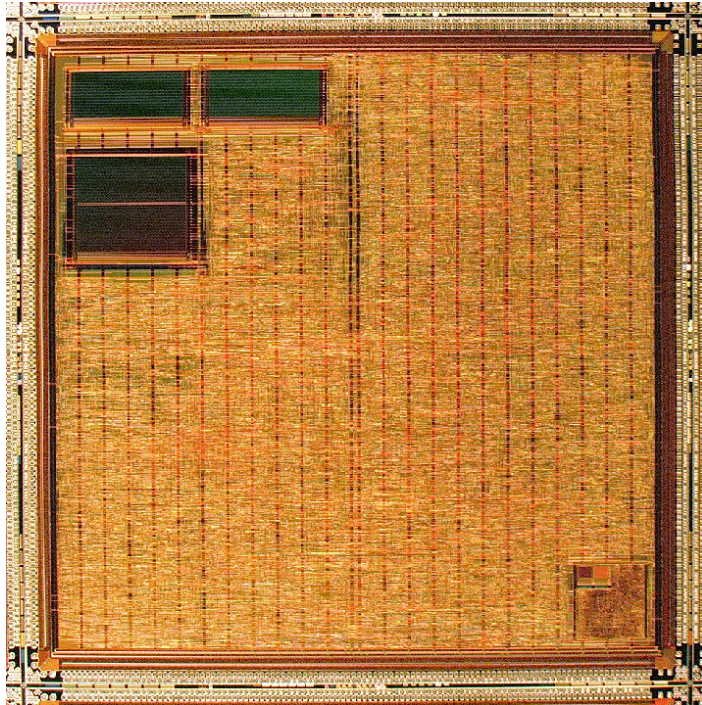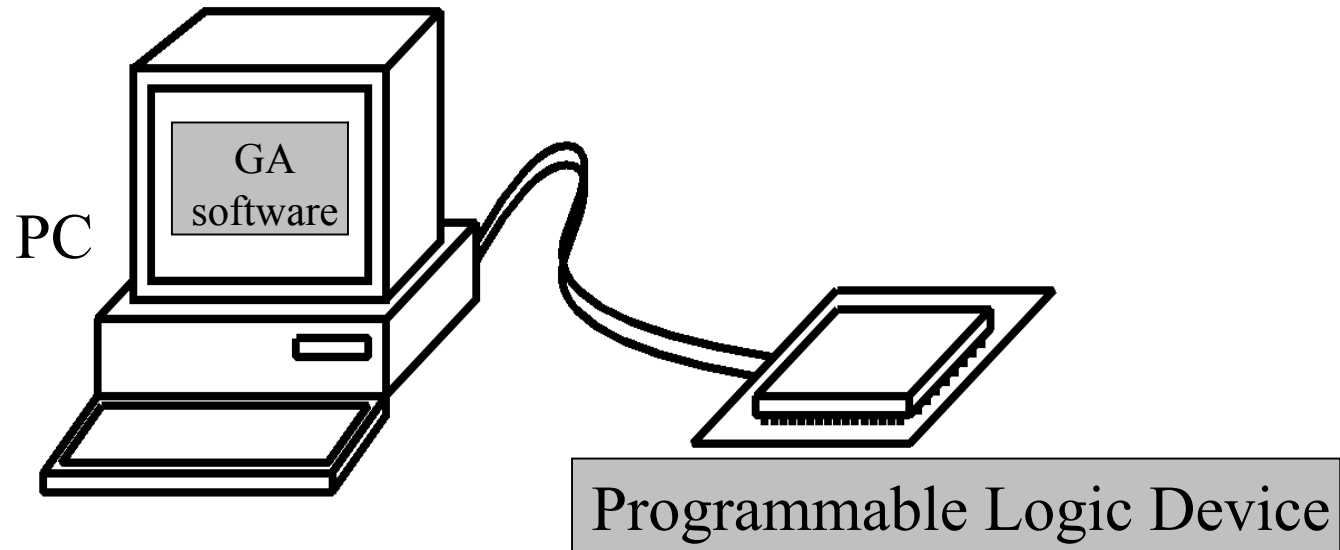
EHW chip

Prosthetic Hand

Problems in conventional EHW

Needs a PC to execute GA $\longrightarrow$ Large Size

Fitness evaluation and GA
by software $\longrightarrow$ Slow Speed

GA
software

PC

Programmable Logic Device

Gate Level EHW Chip

- Integration of GA hardware and a PLA on a single LSI chip

⬇

- Compact & Fast

Convectional EHW

GA

Gate Level EHW chip

GA hardware

PLA

Memory

Interface
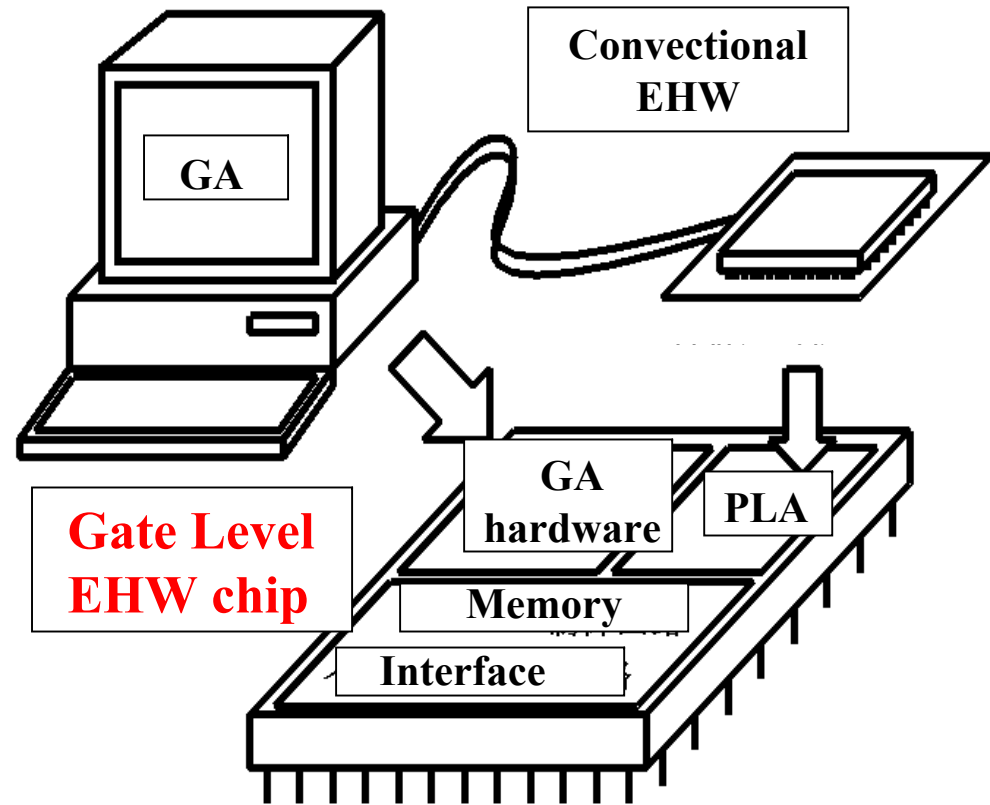
# Myoelectric-controlled prosthetic-hand

- Myoelectric signals
  - Generated from muscular activation.
  - Detected on the surface of the skin by using surface electrode.

- Myoelectric-controlled prosthetic-hand
  - Controlled by myoelectric signals generated from remnant muscles.

Myoelectric signals

Neuron

Myoelectric signals are detected on the surface of the skin by using surface electrode (sensor).

Muscle

Skin

Sensor
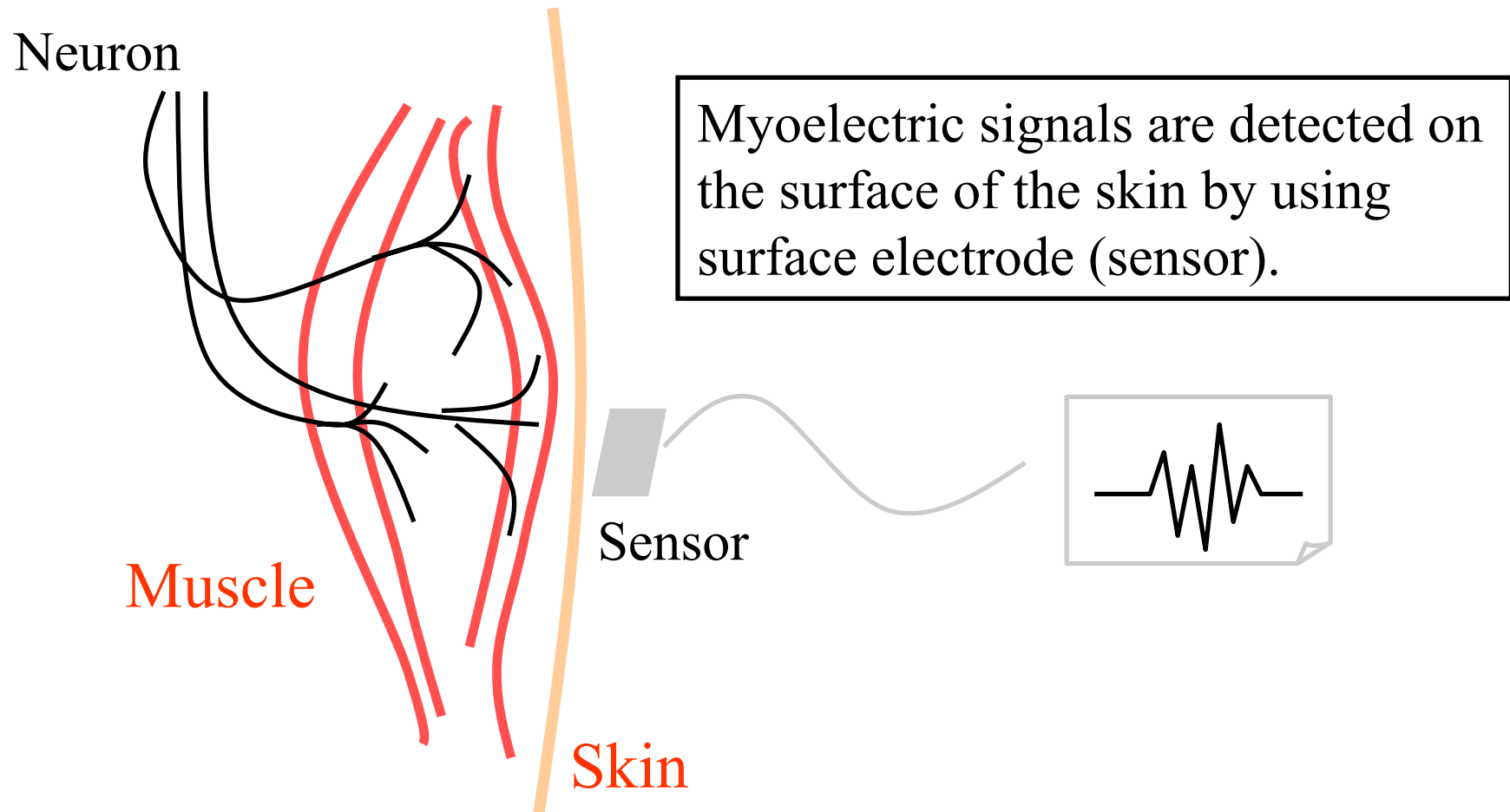
# An example of myoelectric signal patterns
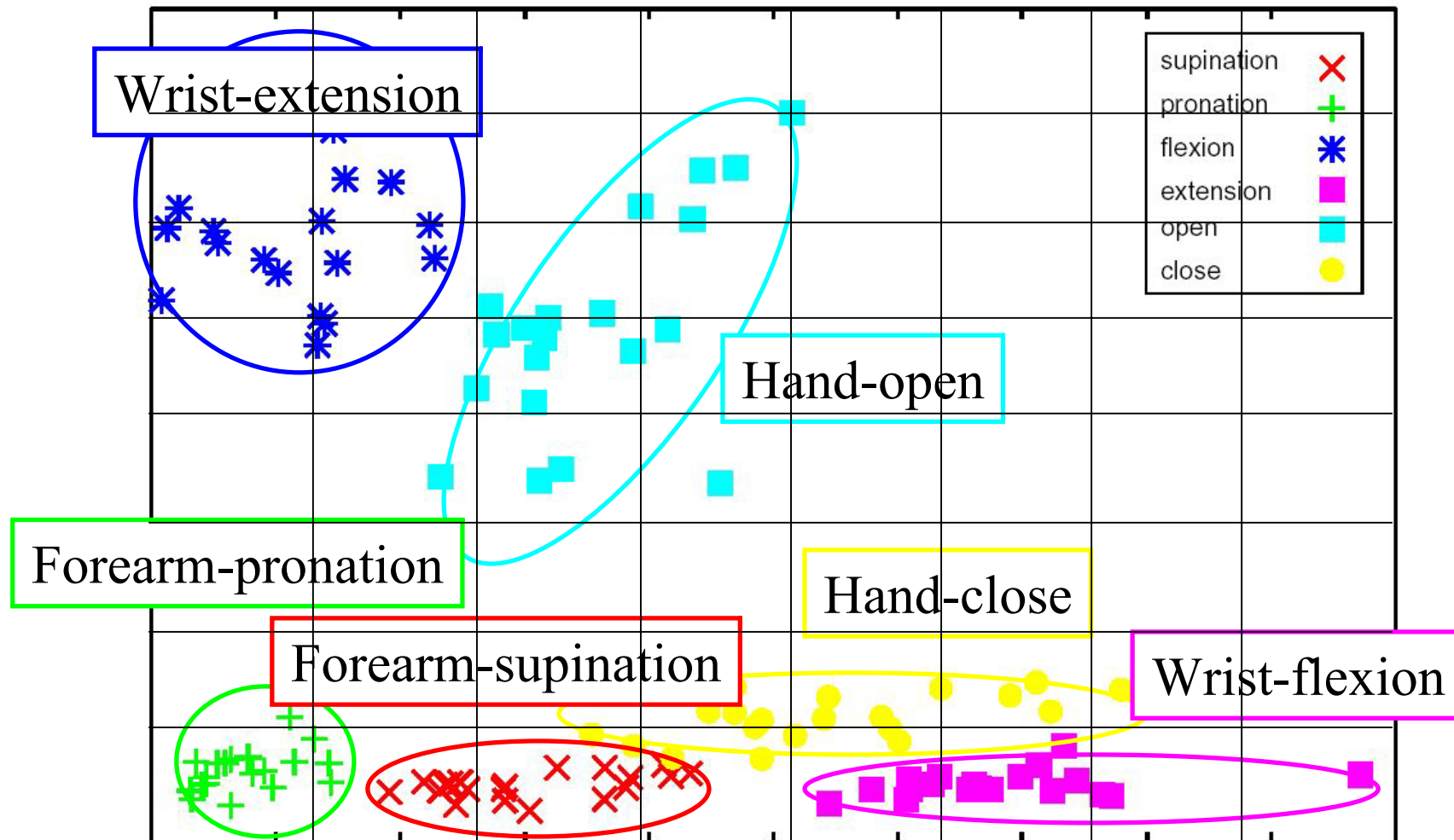
Problems in myoelectric-controllers

- Problem
  - Individuality
    - Characteristics of myoelectric signals differ among individual persons.
    - Difficult to make specification of pattern classification circuit in advance.

- Our solution (1998--)
  - Evolvable hardware
    - An evolvable hardware chip.
    - Programmable hardware + Genetic algorithm
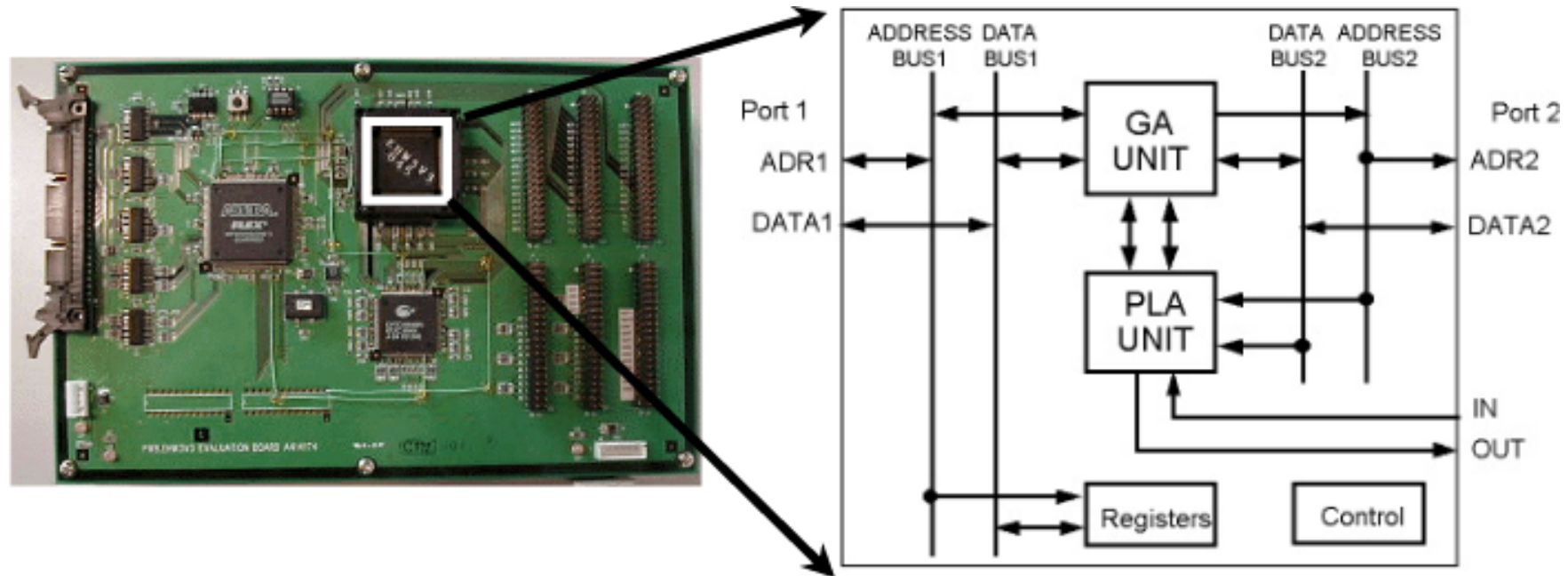
EHW chip architecture

- GA dedicated hardware

- Reconfigurable Hardware (PLA)

- Memory (training data. chromosome)

- Control logic

- Interface

EHW chip (version 1)

Training data Memory

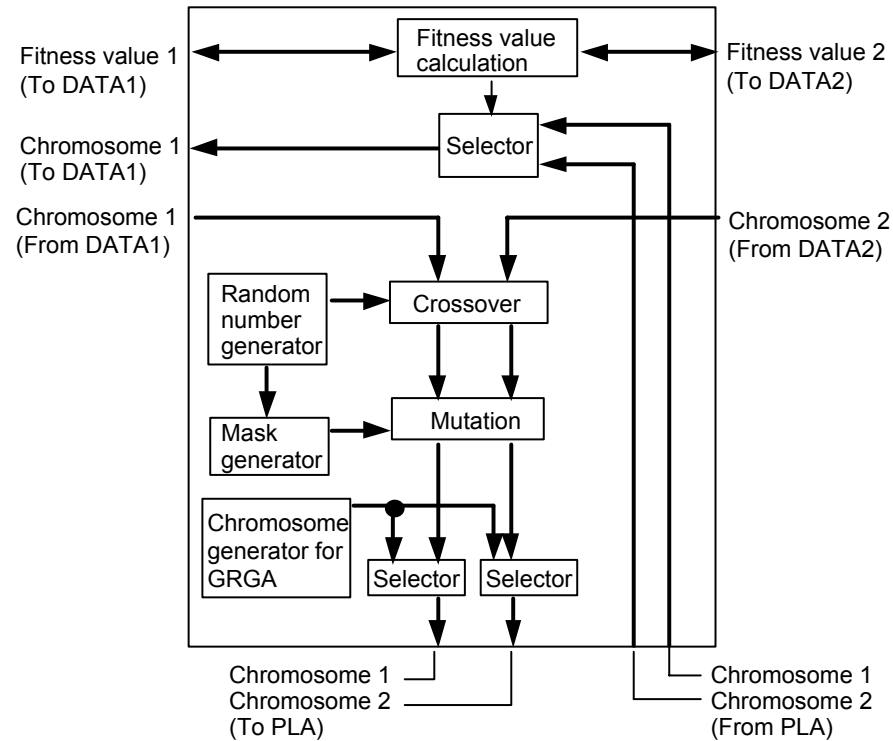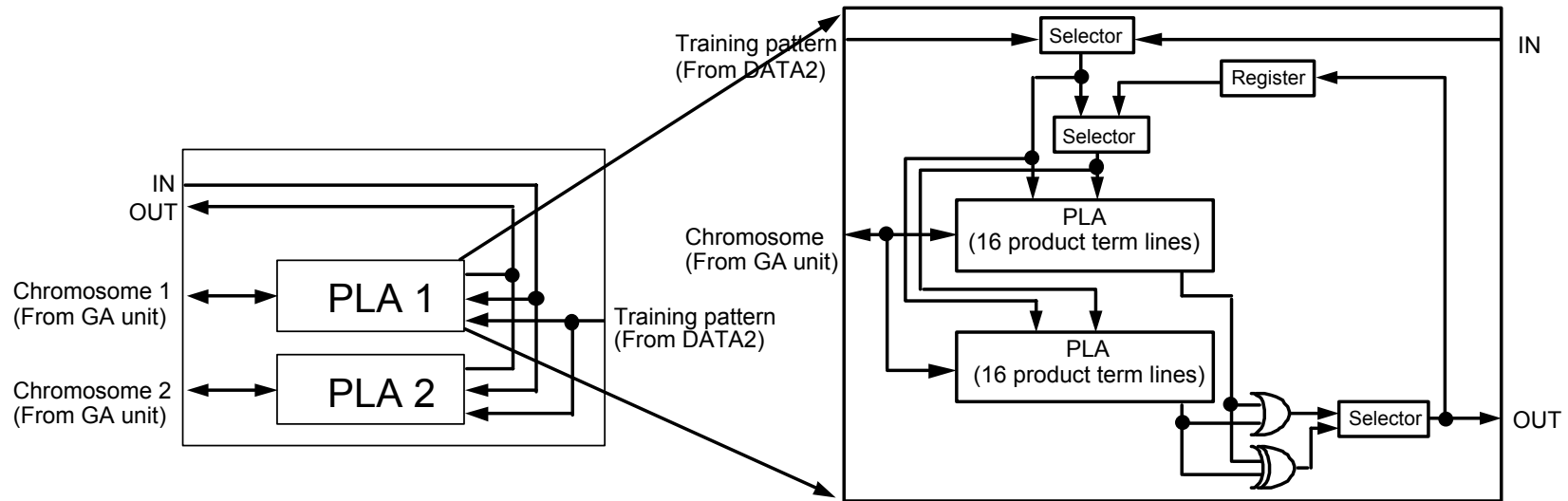Choromome Memory

CPU (V30MX)
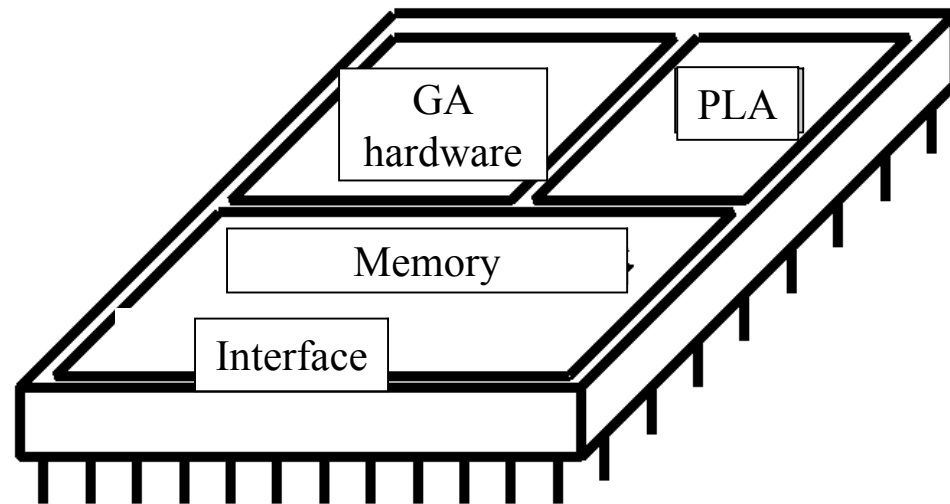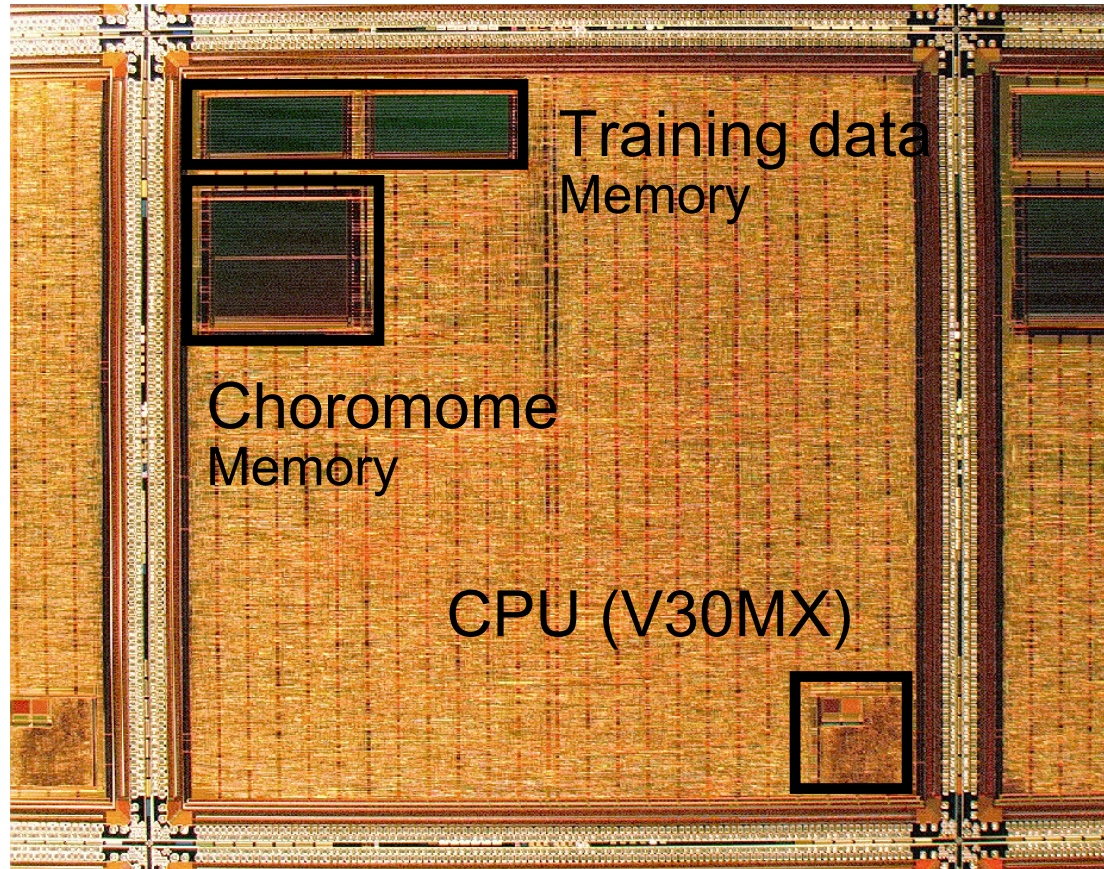
Gate-Level EHW chip

- Package: 144pins QFP, 20x20mm, Cell base LSI.
- Circuit size: about 80,000 gates.
- Clock frequency: 33MHz.

GA Unit

- Steady state GA and uniform crossover are used.
- There are new options for GA. (GRGA, on-line learning etc.)
- Exexution time : 95 us / (chromosome evaluation)
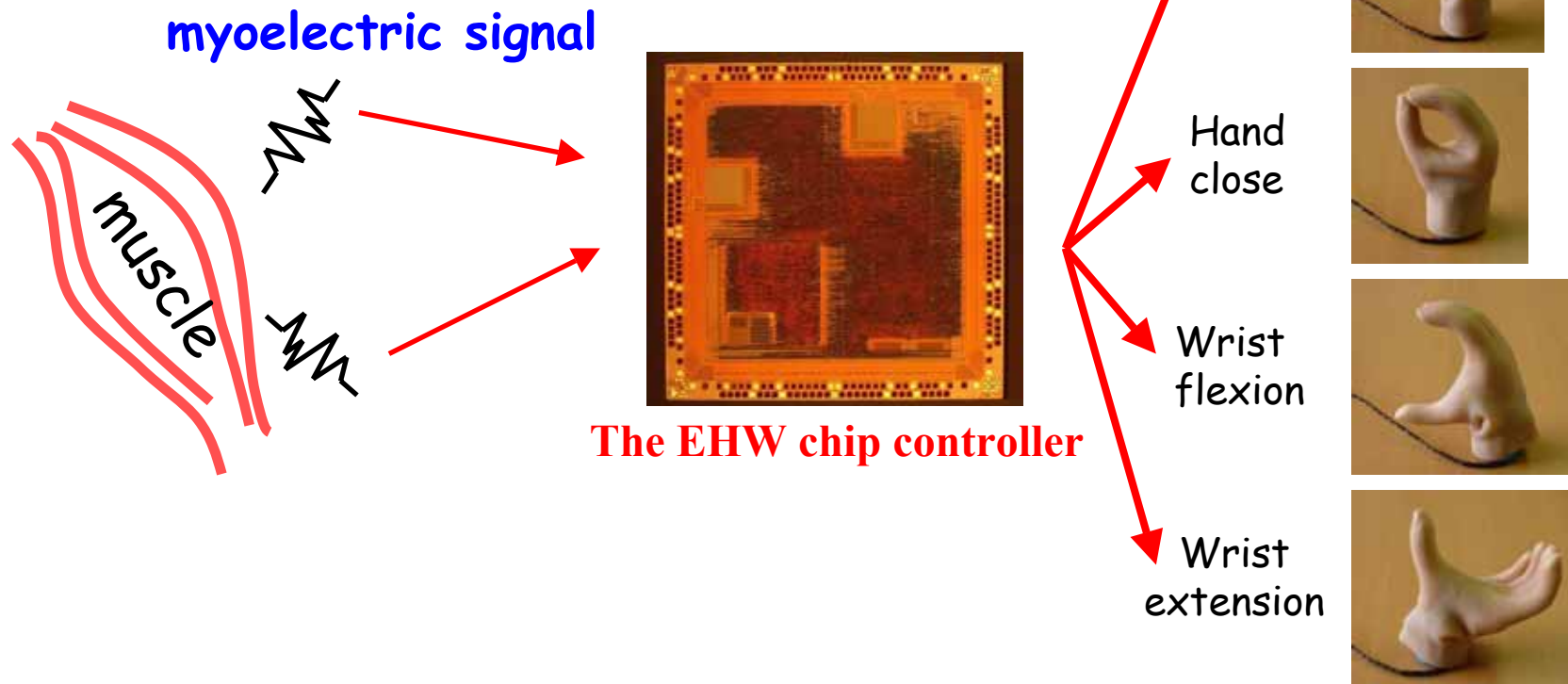 - 40 times faster than software on a PC (1.2GHz).

PLA Unit

- There are two PLAs for parallel evaluation of two circuits.
- I/O: 12bit input / 4bit output, or 8bit input / 8bit output.
- Product term line number: 32 in one PLA.

Performance evaluation

Function	EHW chip (us)	Program (us)	(Program)/(EHW chip)
One evaluation	94.8	3670	38.7
Crossover & mutation	12.6	78.9	6.3
Fitness calculation	68.2	3560	52.2
Comparison of fitness values	0.03	0.15	5.0
PLA execution	0.03	13.42	447.3

- Comparison of the execution time with a GA program on a PC (AMD Athlon CPU 1.2GHz).

=> EHW chip: 38.7 times faster than the program.

   – PLA execution: 447 times faster than the program.

The hand controller with the EHW chip

myoelectric signal

muscle

The EHW chip controller

Hand open

Hand close

Wrist flexion

Wrist extension

Multi-functional myoelectric controlled artificial hand.

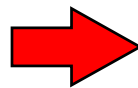| Functions	Hand open-close Wrist flex-extend
Size	almost same as adult human hands
Weight	about 400g
Motor	DC motor X 2
Battery	rechargeable: 12V
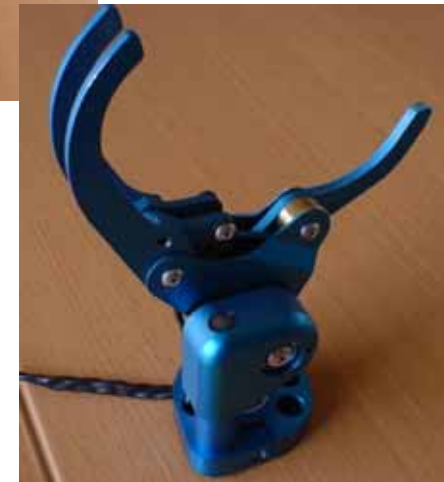
Multi-functional myoelectric controlled artificial hand.

User's merit of multi-functional hand.
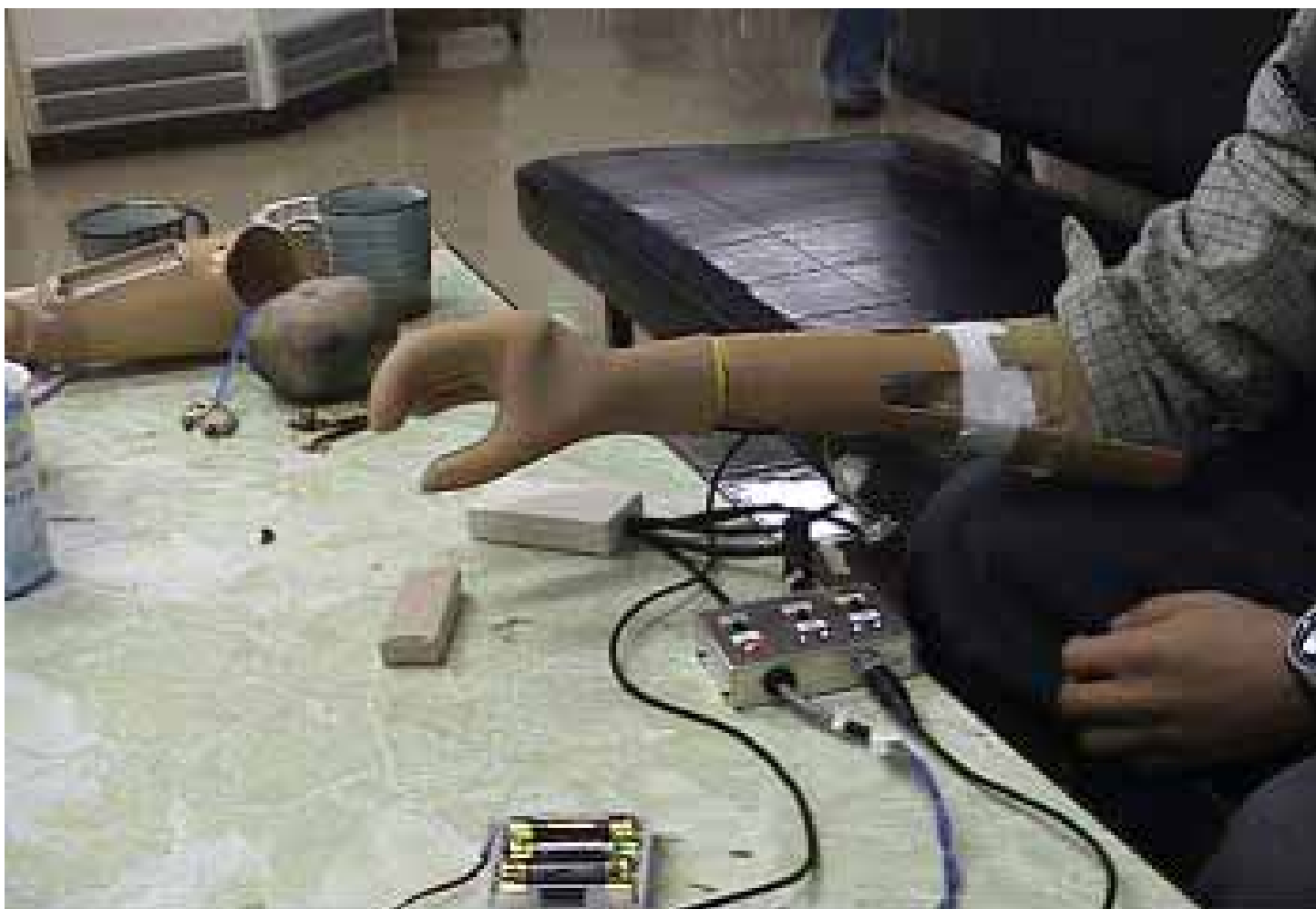
- Natural and easy approach to the object.

**Without wrist flexion.
(Conventional hand)**

With wrist flexion.

Clinical evaluation.

Clock Timing Adjustment

Background

Beyond 90nm, operational yield rate will be degraded
due to process variation.
=> the limit of design capability
=> strong need for post-fabrication LSI adjustment.
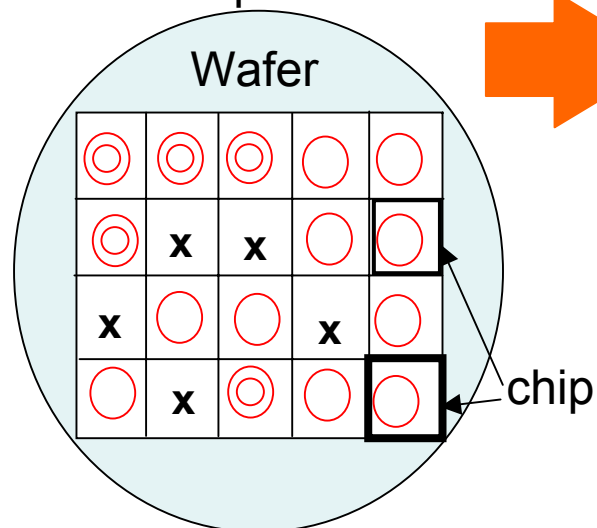
Trend beyond 90 nm:
 from inter-chip variation to intra-chip variation

2001

Tech.node 180nm

Inter-chip variation

Wafer

2003

Tech.node 130nm

Current process

2005~?

Tech.node 90nm

Intra-chip variation

Chip inside
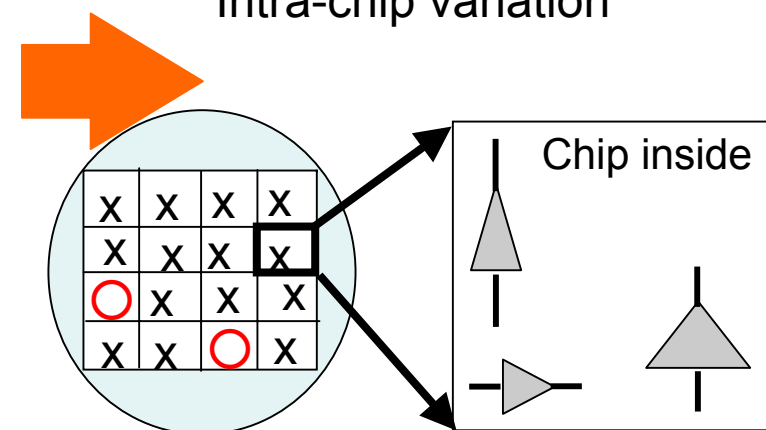
chip

The same logical design no more
guarantees the same performance.

◎ Fast chip   ○ Std. chip   ✗ Bad chip

Our approach: Post-fabrication LSI adjustment

Circuit design including adjustment circuits
+
Fast adjustment software

Fast adjustment software：

Genetic Algorithm(GA) in Artificial Intelligence

GA can determine quickly optimal values of many circuit parameters that affects LSI performance and operational yield rate.

# Genetic algorithm

Genetic Algorithm(GA): A quick and robust search algorithm

step1. Encode multiple circuit parameters into single chromosome.
step2. Define an evaluation function F that decides fitness of chromosomes
        => decision whether a chromosome has good circuit parameters or not.
step3. Prepare multiple chromosomes, then generate better chromosomes with genetic
        operations(e.g. cross-over, mutation) until good circuit parameters are found.

parameter 1   parameter 3   parameter N

0 1 1 0 0 1 1 1 0 ... 1 0 1

N circuit parameteres
are encoded into
single chromosome.

F

F

F
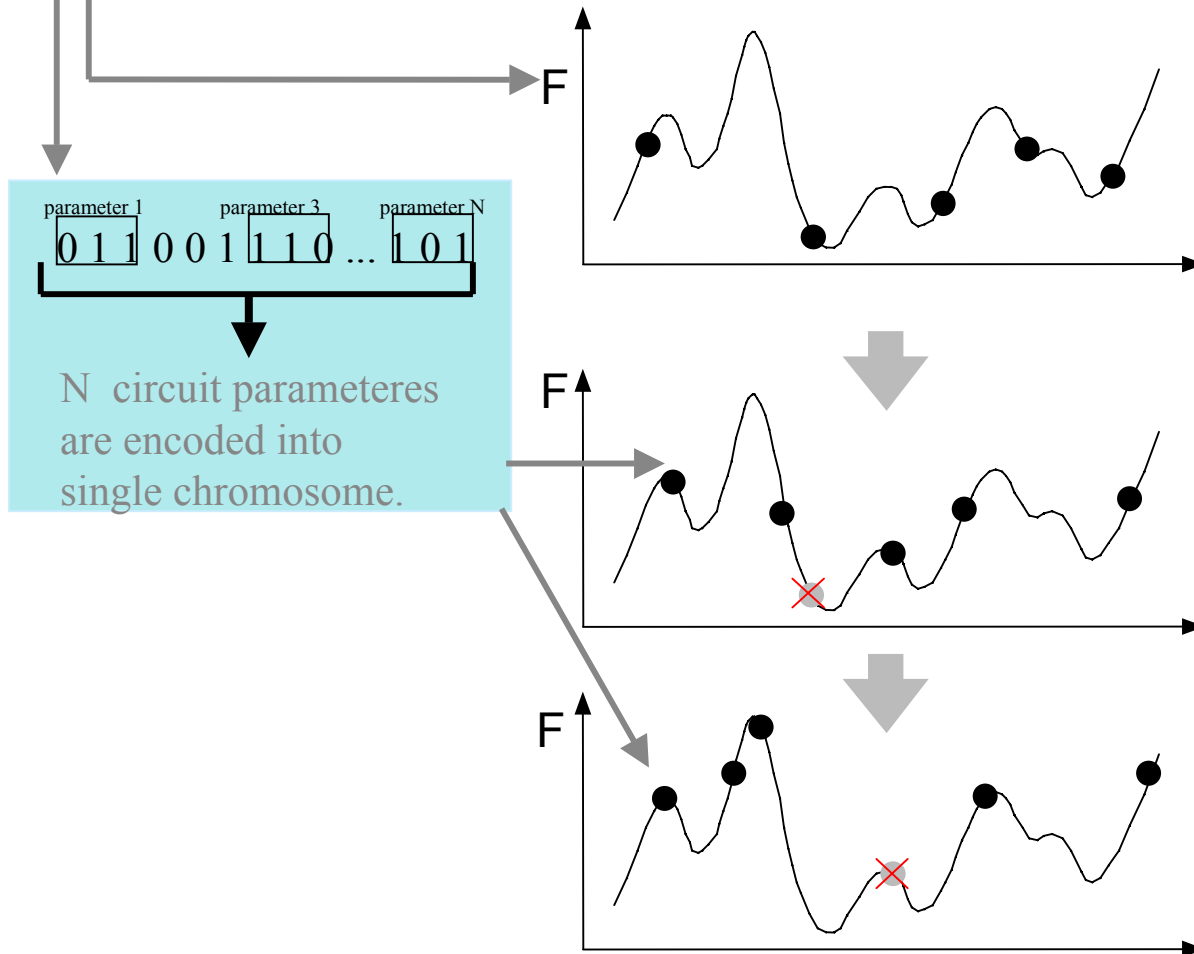
■ **Selection**
- increase high fitness chromosome
- delete low fitness chromosome

■ **Cross-over**
  exchange of chromosomes

101010 1010
000000 0000

101010 0000
000000 1010

■ **Mutation**
  one-bit flip in chromosome
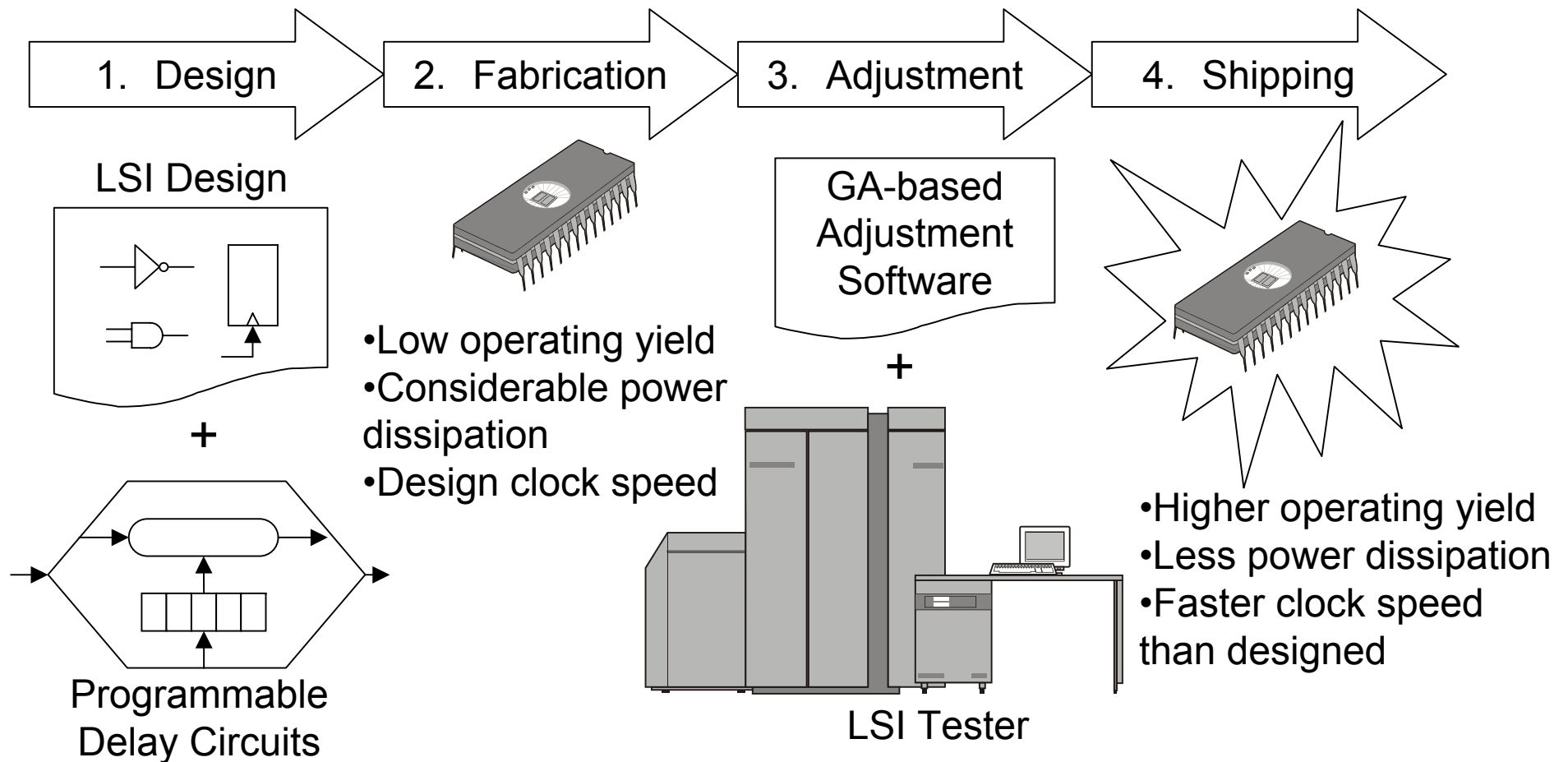
1010101010

1010100010

Outline

- Post-fabrication adjustment for Digital LSI
  - Background & advantages
  - Developed LSIs
  - Results (Three Advantages)
    1. Speed-up of Clock Frequency
    2. Reduction of Power Dissipation
    3. Reduction of Design Time
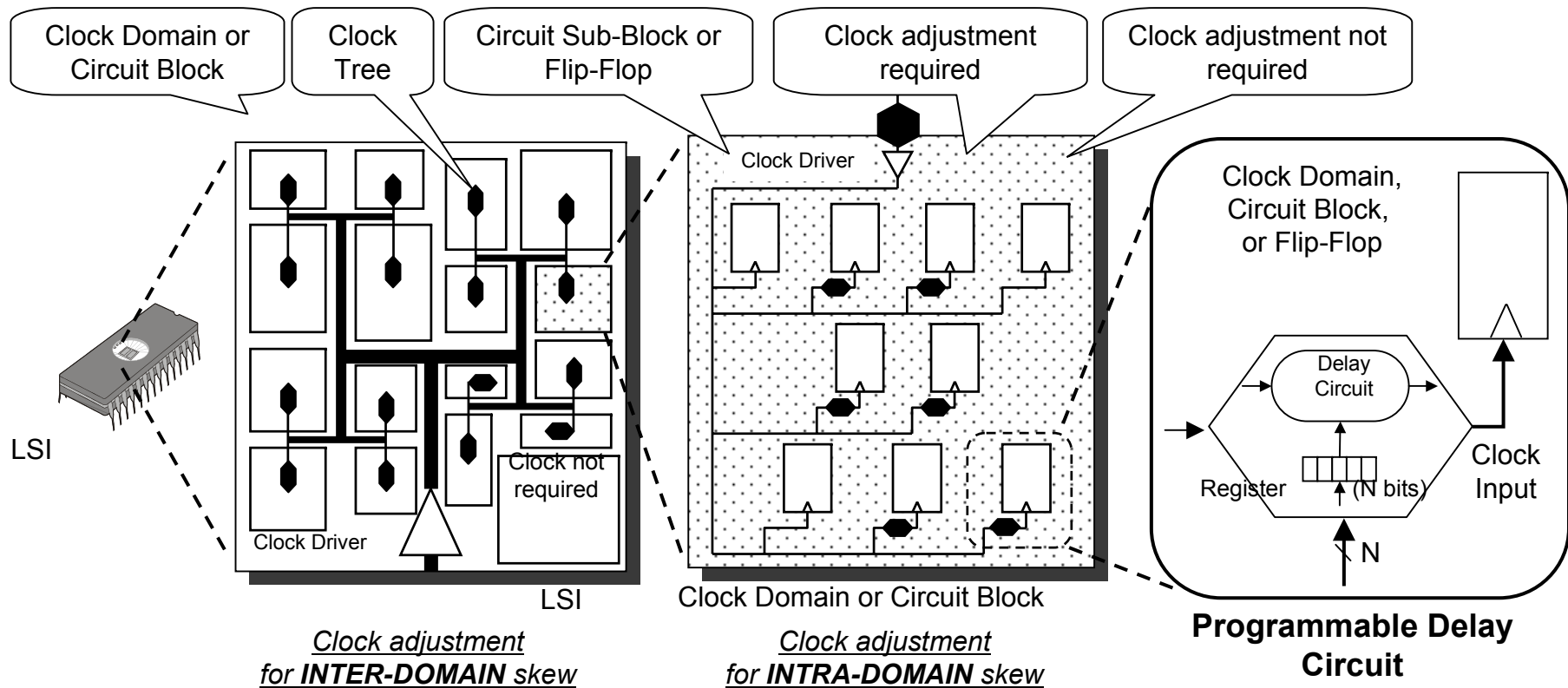
Background & Advantages

- Beyond 90nm, clock skew cannot be avoided only by design due to process variation

- Post-Fabrication clock timing adjustment with Genetic Algorithm

- Two 1GHz LSIs and a design experiment demonstrate three advantages:
  1. Speed-up of Clock Frequency (+25% max)
  2. Reduction of Power Dissipation (-54% max)
  3. Reduction of Design Time (-21% max)

Post-Fabrication Clock Timing Adjustment

1. Design → 2. Fabrication → 3. Adjustment → 4. Shipping

LSI Design

+

Programmable Delay Circuits

• Low operating yield
• Considerable power dissipation
• Design clock speed

GA-based Adjustment Software

+

LSI Tester

• Higher operating yield
• Less power dissipation
• Faster clock speed than designed

Hierarchical Application of Clock Timing Adjustment

Clock Domain or Circuit Block

Clock Tree

Circuit Sub-Block or Flip-Flop

Clock adjustment required

Clock adjustment not required

LSI

Clock Driver

Clock not required

LSI

*Clock adjustment for **INTER-DOMAIN** skew*

Clock Driver

Clock Domain or Circuit Block

*Clock adjustment for **INTRA-DOMAIN** skew*

Clock Domain, Circuit Block, or Flip-Flop

Delay Circuit

Register

(N bits)

Clock Input

N

Programmable Delay Circuit

Clock Skew

(a)   Time t=0

Input Data

Register 1   Circuit A   Register 2   Circuit B   Register 3

5   5   +1   +1
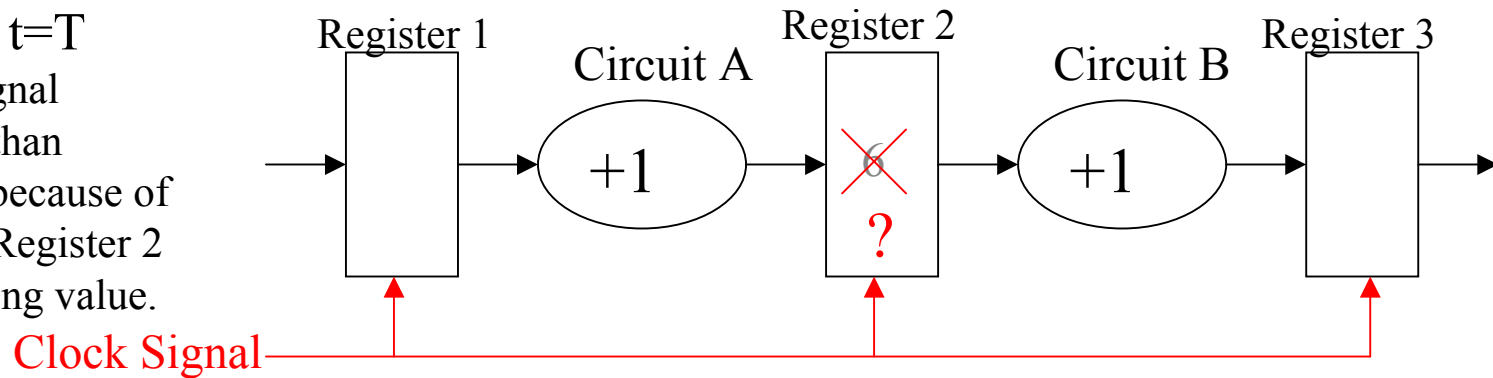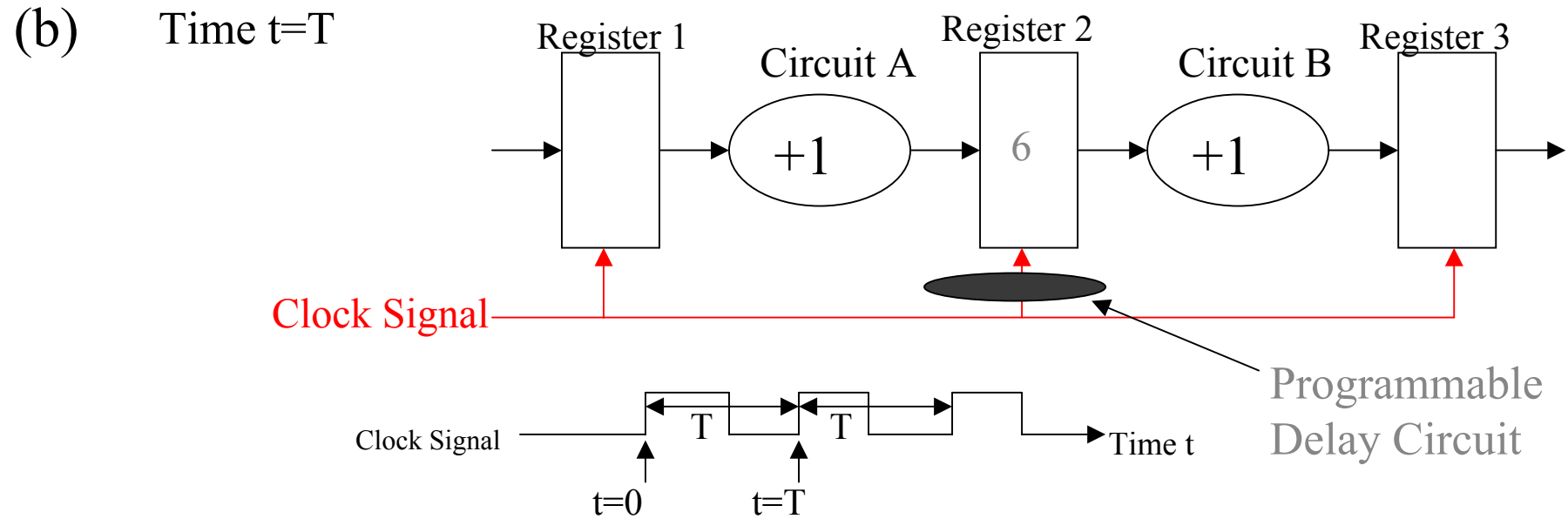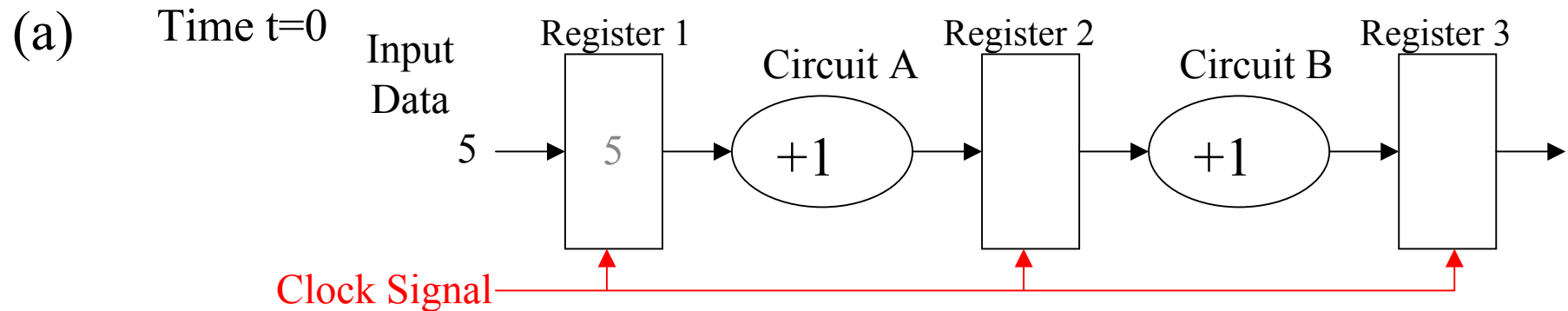
Clock Signal

(b)   Time t=T

When clock signal arrives earlier than specifications because of "clock skew", Register 2 will hold a wrong value.

Register 1   Circuit A   Register 2   Circuit B   Register 3

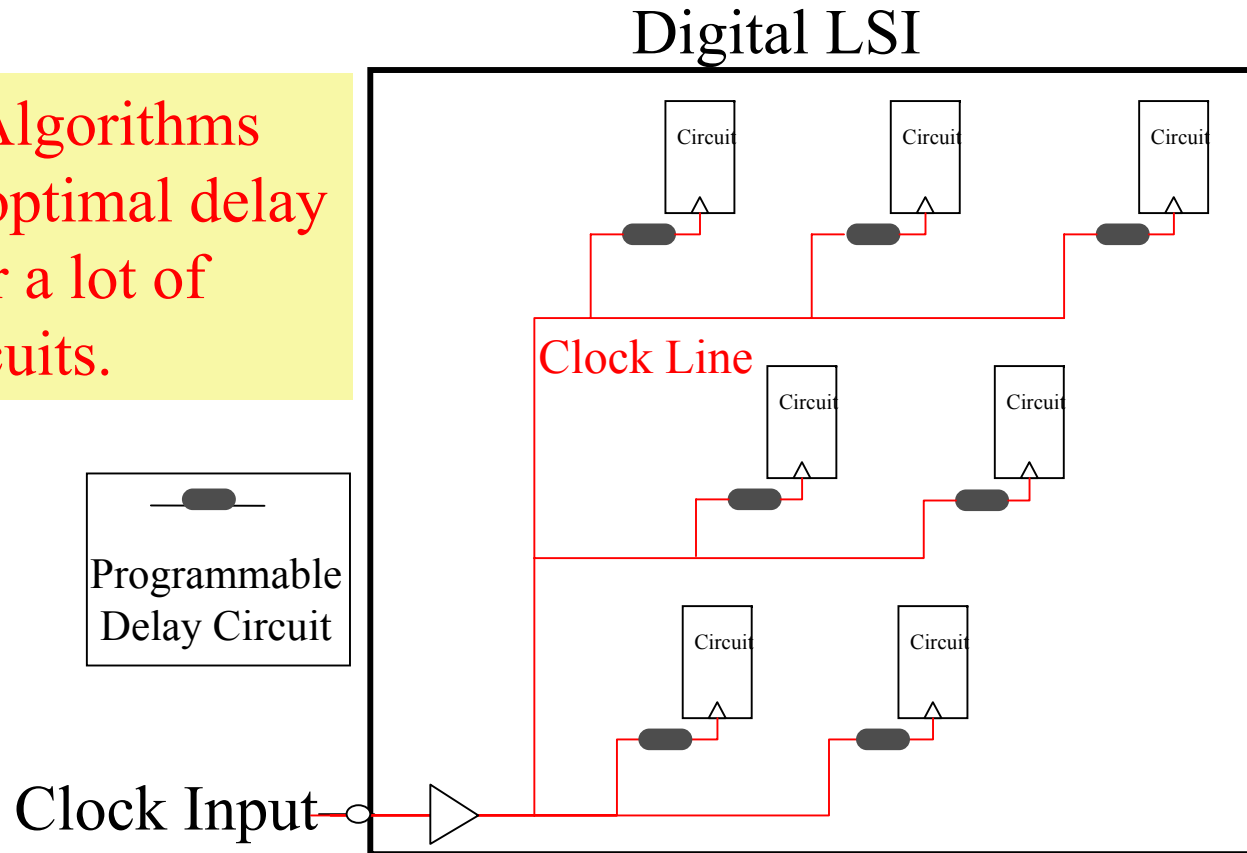+1   6 ?   +1

Clock Signal

Clock Signal   T   T   Time t

t=0   t=T
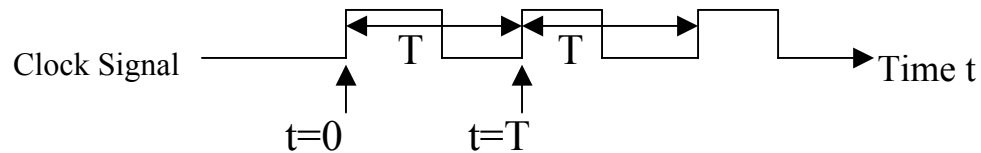
Clock Timing Adjustment for Solving the issues of "Clock Skew"

(a) Time t=0

Input Data

Register 1

Circuit A

Register 2

Circuit B

Register 3

5

5

+1

+1

Clock Signal

(b) Time t=T

Register 1

Circuit A

Register 2

Circuit B

Register 3

+1

6

+1

Clock Signal

Programmable Delay Circuit

Clock Signal

T   T

Time t

t=0   t=T

Insertion of Programmable Delay Circuits

Genetic Algorithms can find optimal delay values for a lot of delay circuits.
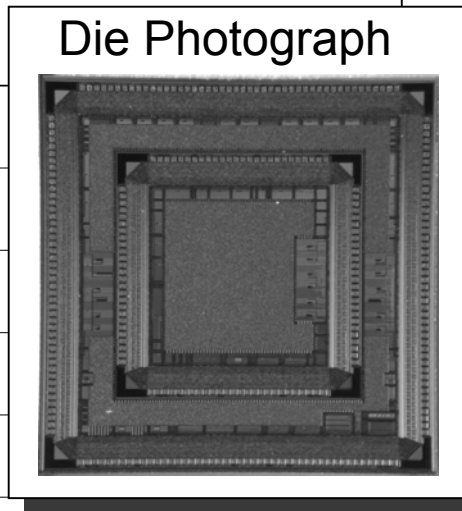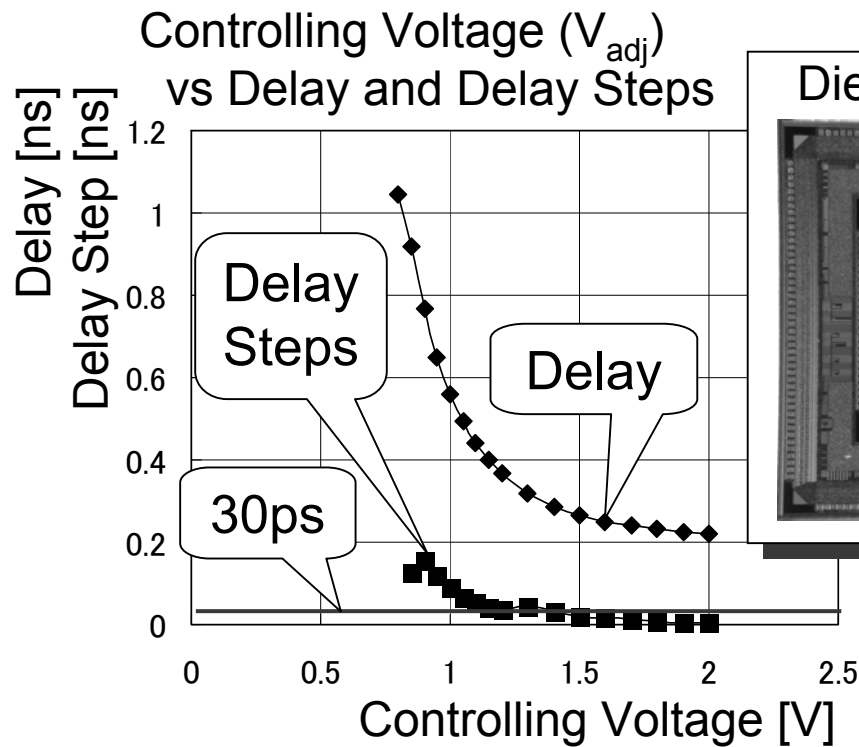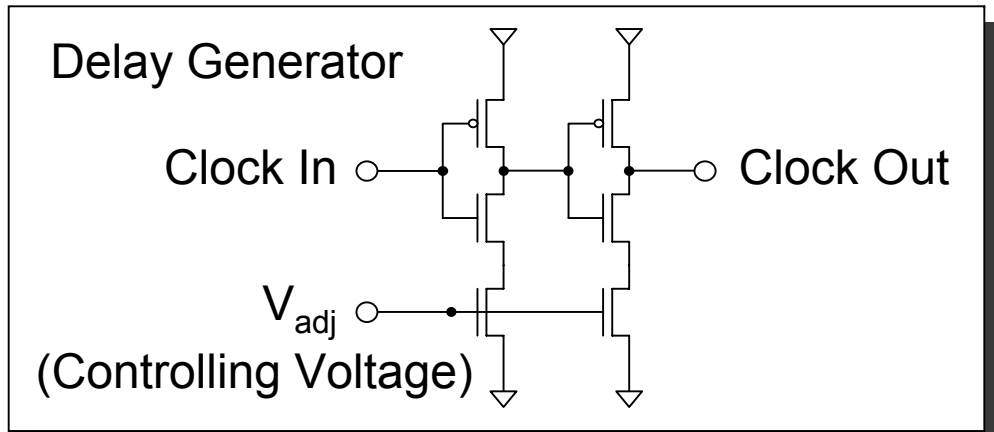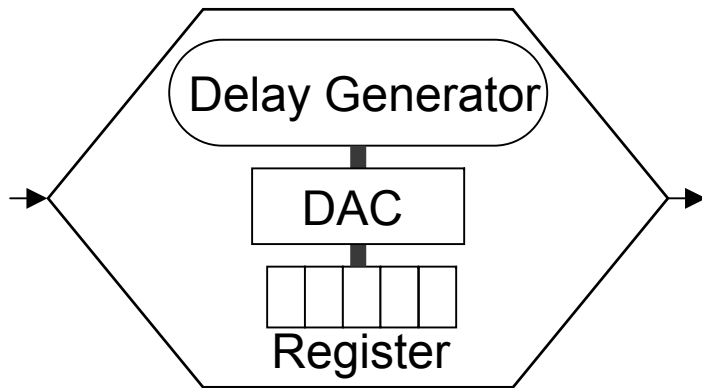
Digital LSI

Circuit

Circuit

Circuit

Clock Line

Circuit

Circuit

Programmable Delay Circuit

Circuit

Circuit

Clock Input

Delay Values must be globally optimized!

Programmable Delay Circuit

Delay Generator

DAC

Register

Delay Generator

Clock In ○ — Clock Out

V_{adj} ○
(Controlling Voltage)

DAC (Digital-Analog Converter)

P·A
$\overline{P}$·A
A
$\overline{A}$
$\overline{P}$·A

P·B
$\overline{P}$·B
B
$\overline{B}$
$\overline{P}$·B

P·C
$\overline{P}$·C
C
$\overline{C}$
$\overline{P}$·C

V_{ref}

V_{out}
(to V_{adj})

Die Photograph

Controlling Voltage (V_{adj})
vs Delay and Delay Steps

Delay [ns]   Delay Step [ns]

Delay Steps

Delay

30ps

Controlling Voltage [V]
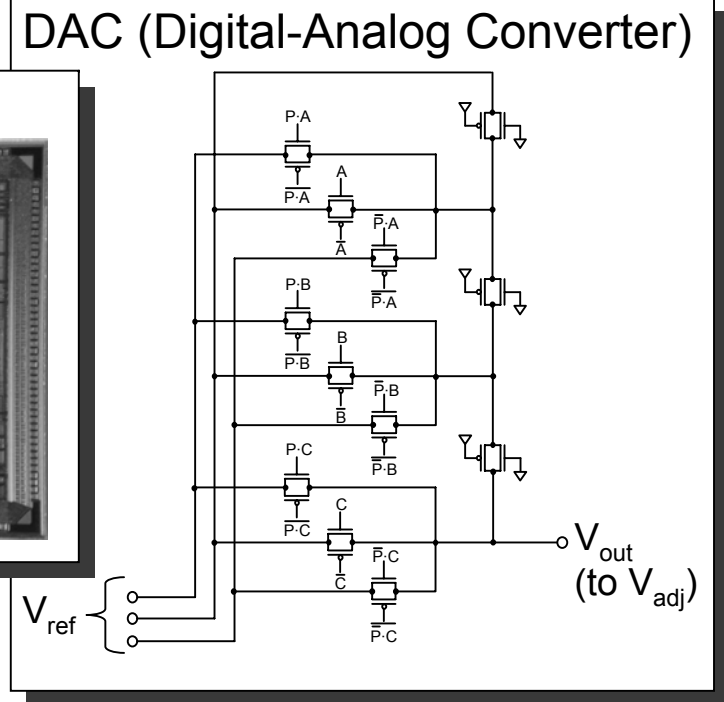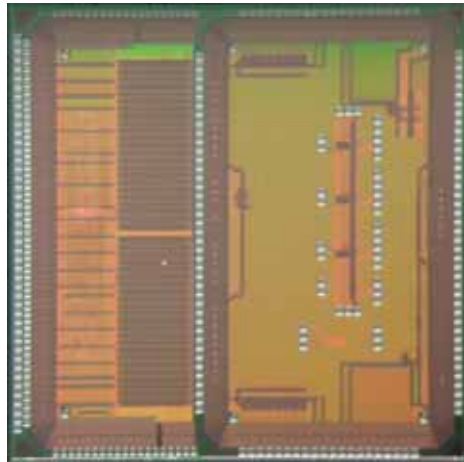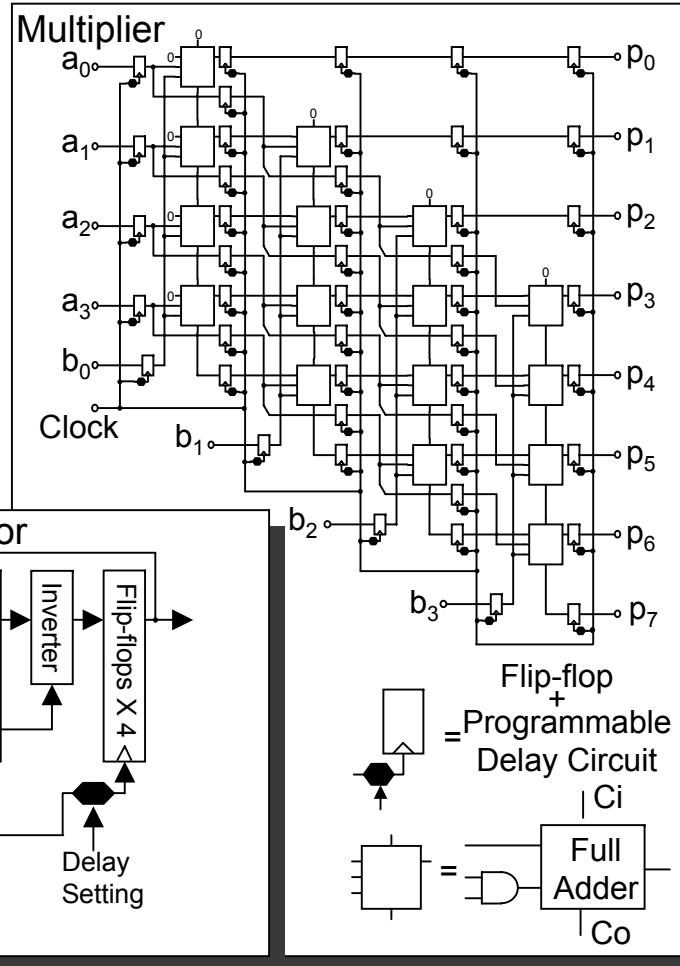
"Delay Steps" are calculated as differences between adjacent delay plots.

- 0.18um, CMOS process
- 18Tr: Delay Generator + DAC
- Some Delay Steps are less than 30ps

Test Chip No.2: Multiplier and Memory Test Pattern Generator

Die Photograph

Multiplier

a_0 a_1 a_2 a_3 b_0

Clock b_1 b_2 b_3

p_0 p_1 p_2 p_3 p_4 p_5 p_6 p_7

Flip-flop
+
Programmable
Delay Circuit

Ci

Full
Adder

Co

Memory Test Pattern Generator

Flip-flops X 9 — Decoder — Flip-flops X 9 — ALU — Flip-flops X 5 — Inverter — Flip-flops X 4

Clock
Input

Delay
Setting

Delay
Setting

Delay
Setting

Delay
Setting

Programmable Delay Circuit

0.13um, CMOS process, Design for 1GHz(typ),
Using the "Programmable Delay Circuits"
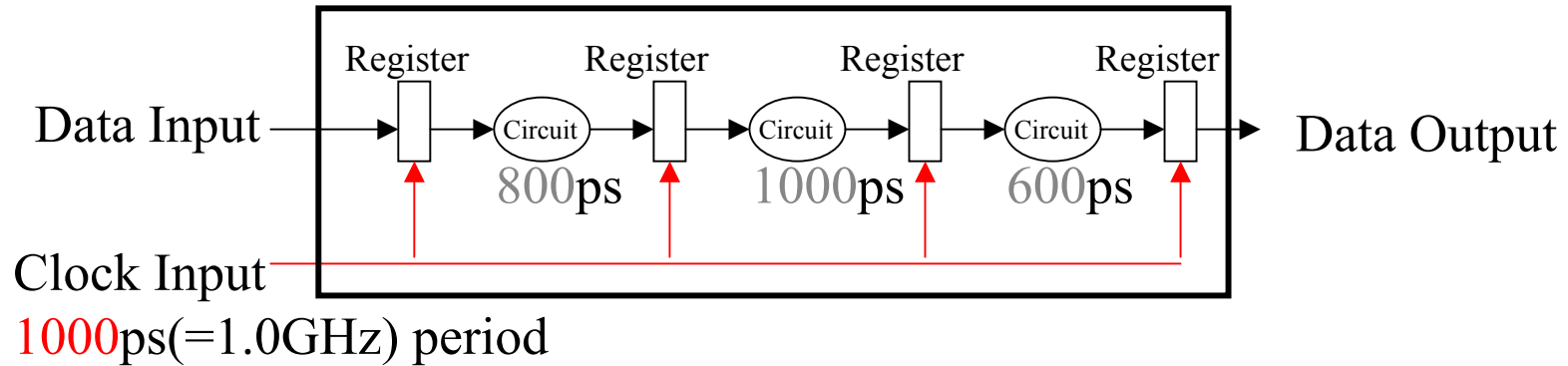
Three Advantages of GA-based adjustment

1.Speed-up of Clock Frequency (+25%)

2.Reduction of Power Dissipation (-54%)
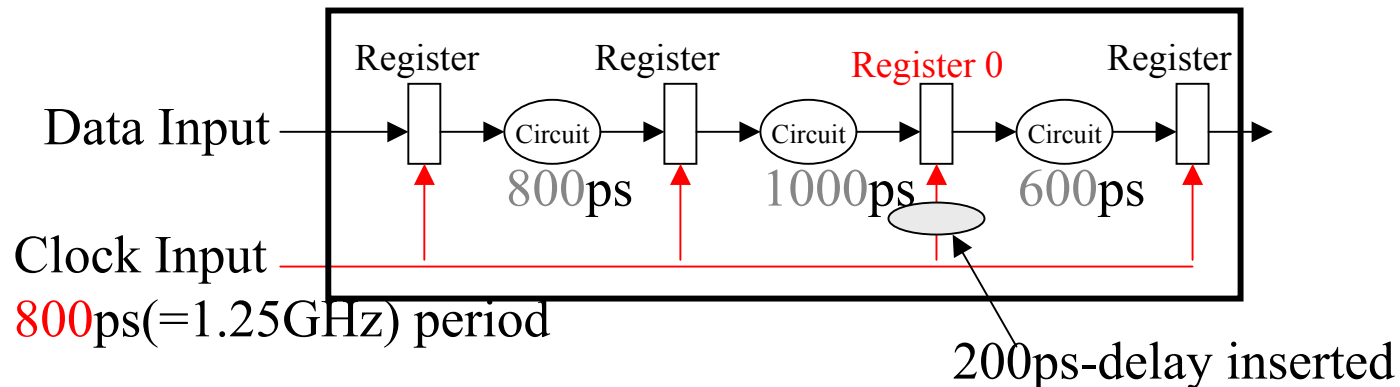
3.Reduction of Design Time (-21%)

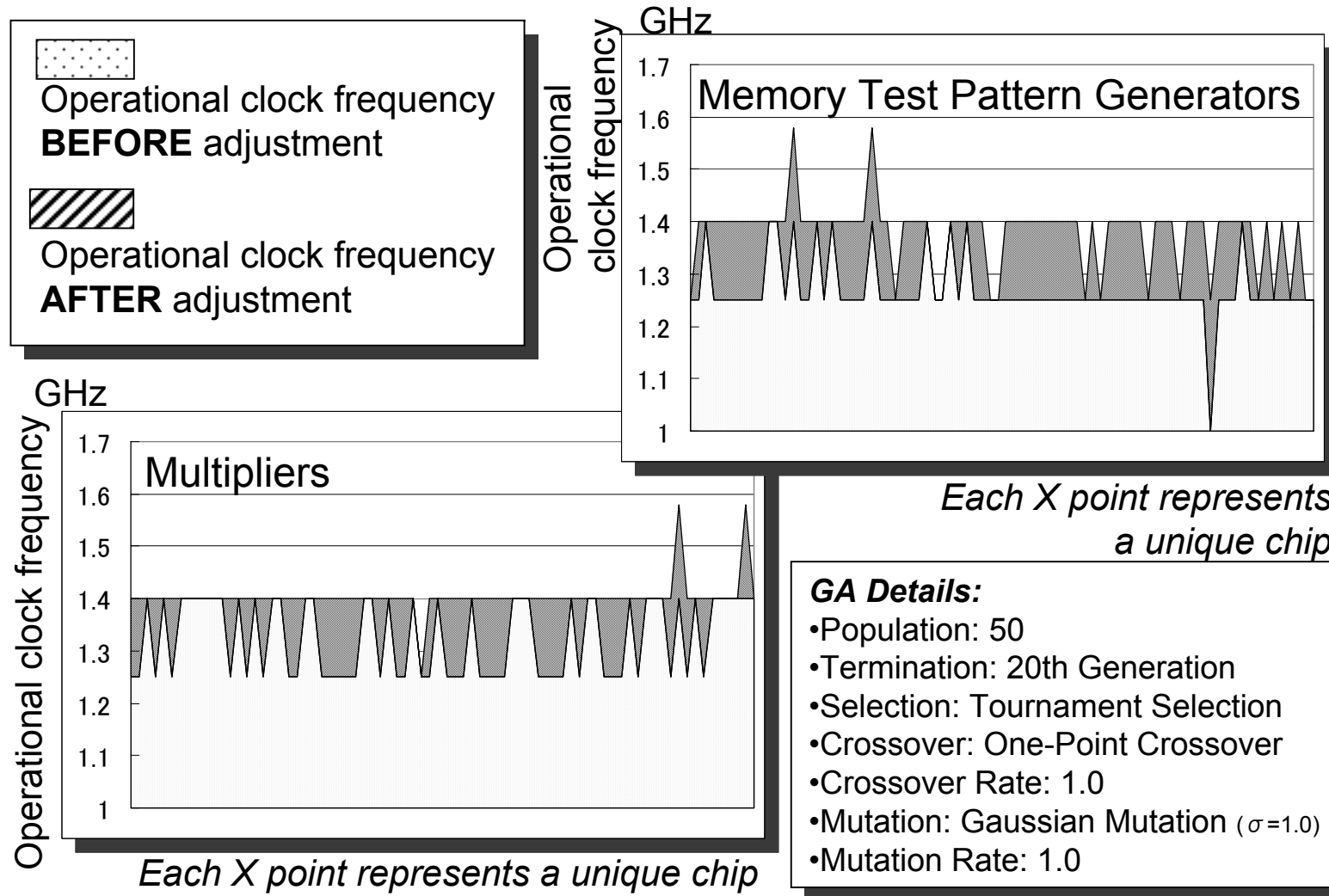# Advantage No.1: Clock Frequency Speed-up

LSI : Designed at 1000ps(=1GHz) period

Data Input

Register Register Register Register
Circuit 800ps Circuit 1000ps Circuit 600ps

Data Output

Clock Input
1000ps(=1.0GHz) period

25% Enhancement
of Clock Frequency
(1000/800=1.25)

LSI : Clock period is enhanced to 800ps(=1.25GHz)

Data Input

Register Register Register 0 Register
Circuit 800ps Circuit 1000ps Circuit 600ps

Clock Input
800ps(=1.25GHz) period

200ps-delay inserted

Experiment Result:
Clock Frequency Speed-up

Operational clock frequency **BEFORE** adjustment

Operational clock frequency **AFTER** adjustment

GHz

Operational clock frequency

Memory Test Pattern Generators

1.7
1.6
1.5
1.4
1.3
1.2
1.1
1

GHz

Operational clock frequency

Multipliers

1.7
1.6
1.5
1.4
1.3
1.2
1.1
1

Each X point represents a unique chip

Each X point represents a unique chip

GA Details:
- Population: 50
- Termination: 20th Generation
- Selection: Tournament Selection
- Crossover: One-Point Crossover
- Crossover Rate: 1.0
- Mutation: Gaussian Mutation (σ =1.0)
- Mutation Rate: 1.0

25% increase over all the chips

Advantage No.2: Power Supply Voltage Reduction

LSI which operates at standard power supply voltage 1.2V

Register   Register   Register   Register   Register

Data Input

Data Output

Clock Input
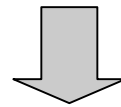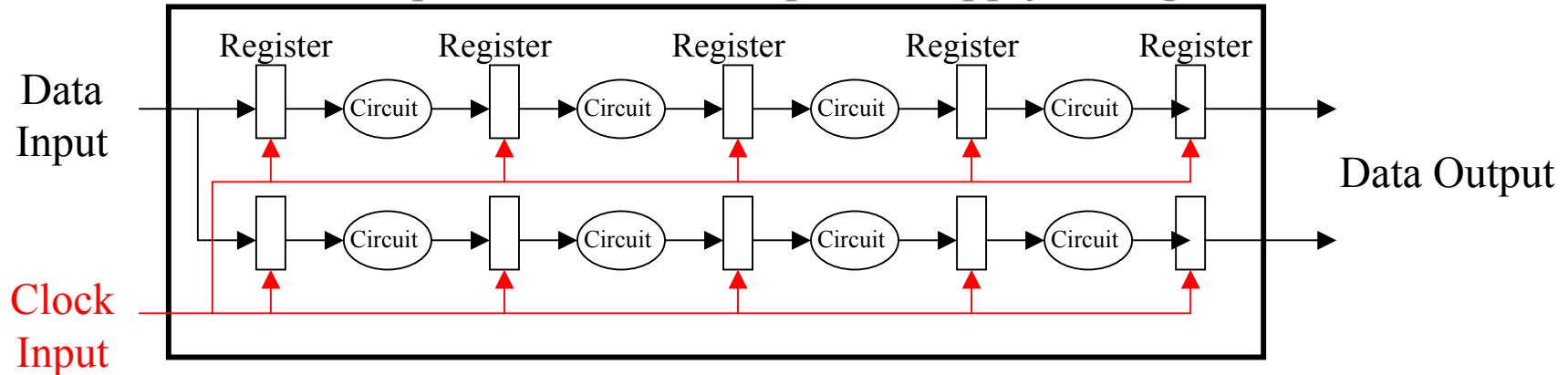
Lowering power supply voltage, from 1.2V to 0.8V

LSI which operates at lower power supply voltage 0.8V

Register   Register   Register   Register   Register

Data Input

Data Output

Clock Input

Circuits which violate timing constraints

Programmable Delay Circuit
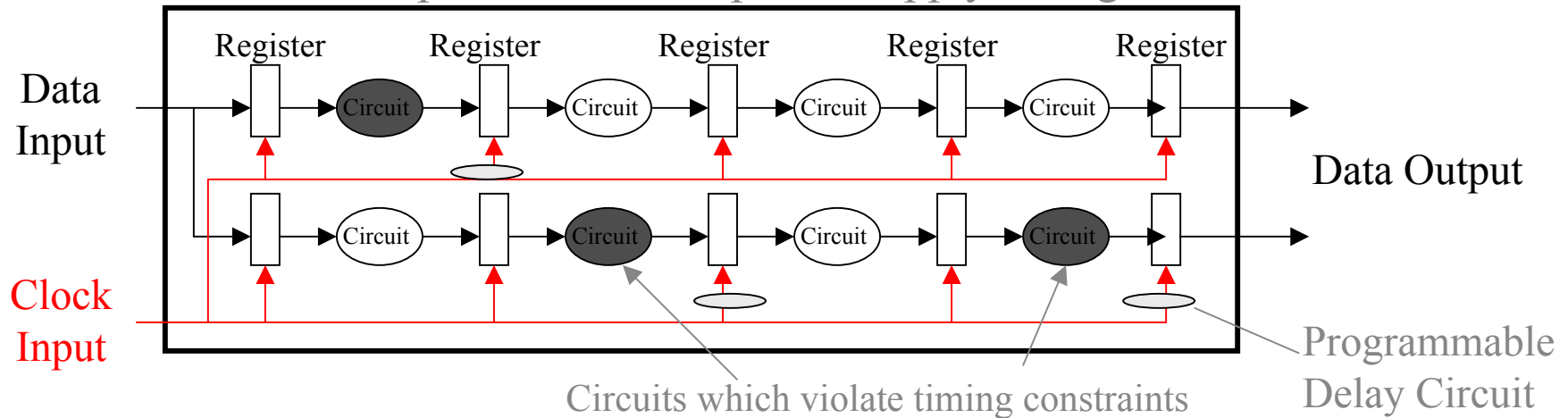
Experiment Result:
Power Supply Voltage Reduction

Operational yield at each voltage and
clock frequency, **BEFORE** adjustment

	0.8V	0.9V	1.0V	1.1V	1.2V
1.58GHz	0%	0%	0%	0%	0%
1.4GHz	0%	0%	20%	30%	40%
1.25GHz	② 0%	40%	100%	100%	① 100%
1.0GHz	100%	100%	100%	100%	100%

Clock ⇩ Adjustment

Operational yield at each voltage and
clock frequency, **AFTER** adjustment

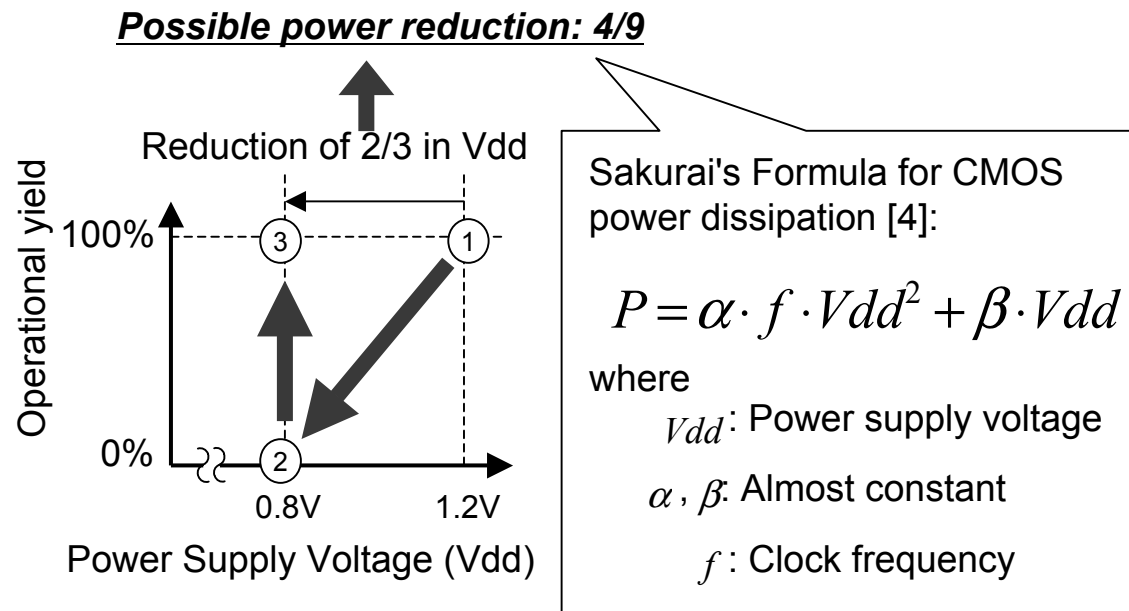|	0.8V	0.9V	1.0V	1.1V	1.2V
1.58GHz	0%	0%	10%	20%	10%
1.4GHz	30%	60%	80%	100%	90%
1.25GHz	③ 100%	100%	100%	100%	100%
1.0GHz	100%	100%	100%	100%	100%

Voltage: 1.2V
⇩
0.8V

&
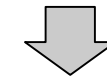
Frequency: 1.0GHz
⇩
1.25GHz

Measured with the Memory-test-pattern Generators.

Experiment Result:
Power Dissipation Reduction

Possible power reduction: 4/9

Reduction of 2/3 in Vdd

Sakurai's Formula for CMOS power dissipation [4]:

$$P = \alpha \cdot f \cdot Vdd^2 + \beta \cdot Vdd$$

where

Vdd : Power supply voltage

α , β: Almost constant

f : Clock frequency

① ② ③ correspond to the same marks in Fig. 3

Reduction of 2/3 in Vdd: 1.2V ⟶ 0.8V

Power Reduction: 4/9 (-54%)

Results: -75% !

Advantage No.3:
Design Time Reduction

Target Design: DDR-SDRAM controller circuit

Design Stage	Traditional [1]	GA-based [1]
Function Design	12.0	**1.5**
Logic Design	30.0	30.0
Floor Planning	7.0	**2.0**
Verification (1)	5.0	5.0
Layout Design	7.0	**1.5**
Verification (2)	6.0	**4.0**
Library Design	42.0	42.0
Total	109.0 ⟶	86.0

*1 day*person

-21%

Overhead of the post-fabrication GA adjustment:

1. Area Overhead   4%

2. Time for Clock Timing Adjustment

Operations	Time (s)
Generation of Delay Setting and Test Data for Function Test	0.55
Write Data to Chip	0.02
Execution of Test	0.01
Read Results of Test from Chip	0.03
Calculation of Fitness	0.33
Total Time	**0.94**

Lossless compression method
for very high-resolution image data

Overview

- **Lossless** compression method bi-level image with high-resolution.

- Amendment to JBIG2 standard.

  (ISO/IEC JTC1/SC29/WG1 France meeting, 2003)

  - JBIG2 = **J**oint **B**i-level **I**mage experts **G**roup, **2**

    - International standard for bi-level image coding
    - ISO/IEC 14492 | ITU-T T.88

- Activity toward incorporating JBIG2-AMD2 datastream into TIFF/IT

  - TIFF/IT = **T**ag **I**mage **F**ile **F**ormat for **I**mage **T**echnology

    - International standard of graphic data format for data exchange
    - ISO 12639

Digitalization of Workflow in Graphic-Arts Industry
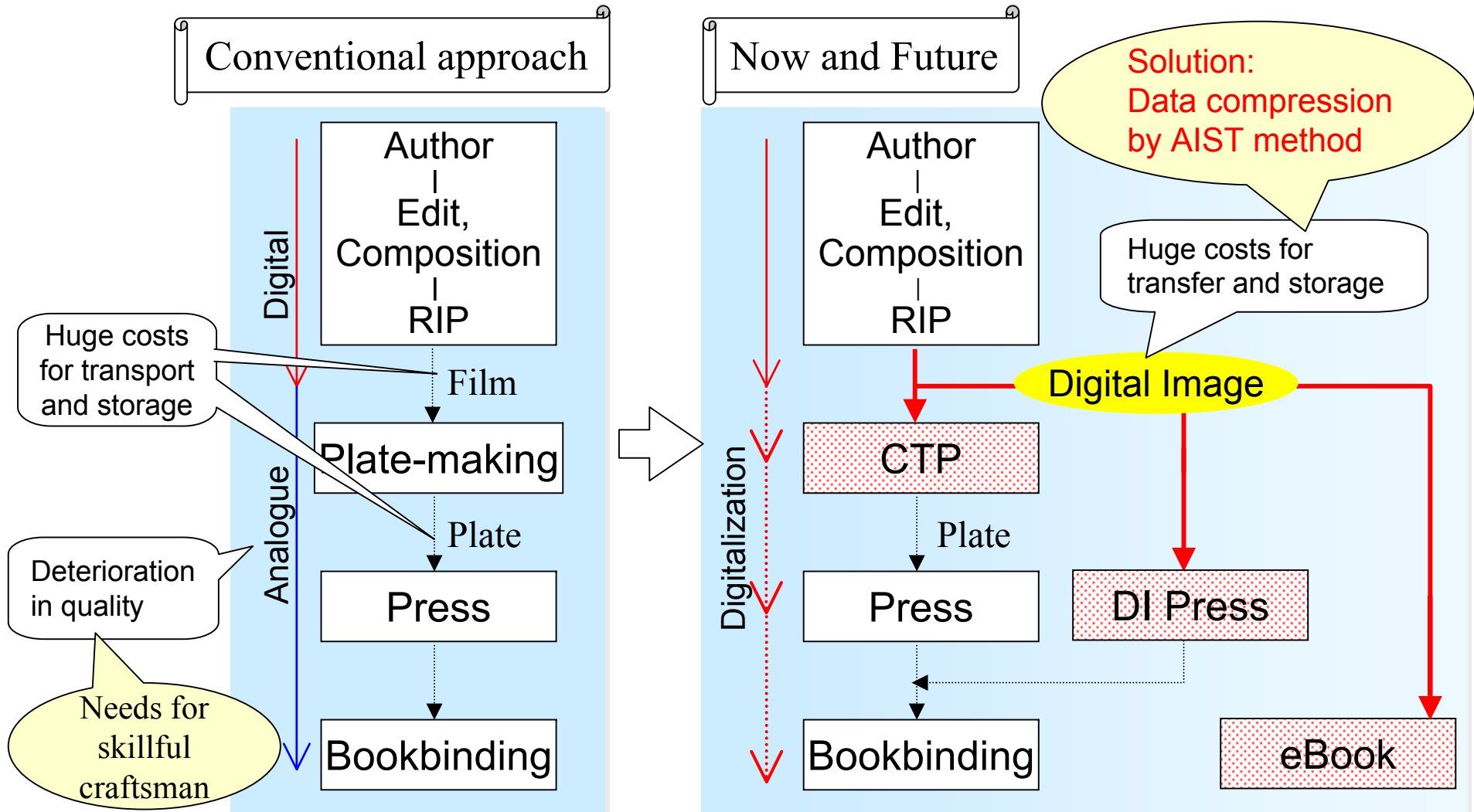
High-resolution Image for Graphic-Arts

Color Image

RIP
Raster Image Processor

Press

Graphic-Arts Image
- Bi-level
- Very-high resolution

High quality printed material
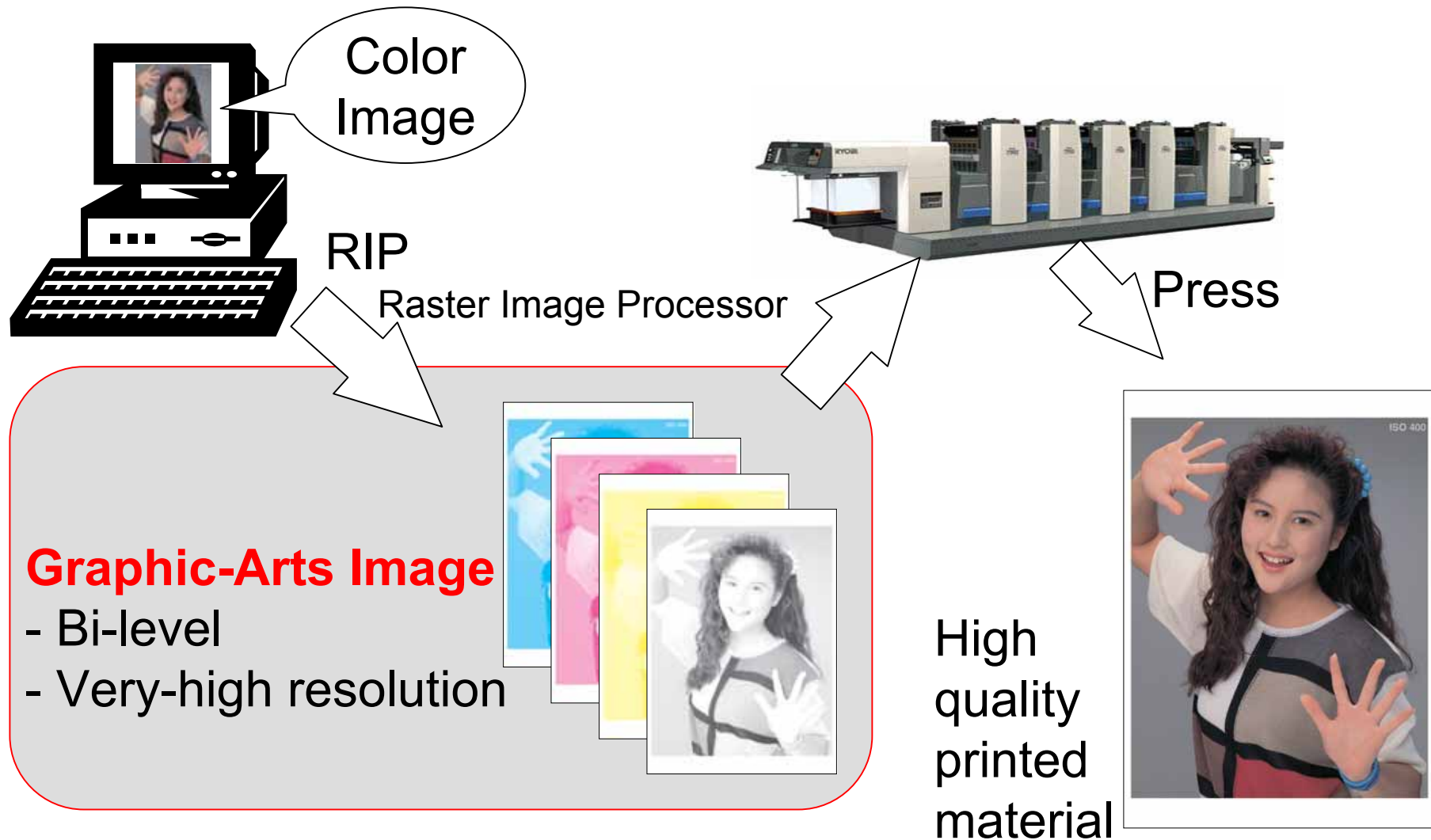
Lossless Compression of JBIG2

256 pixels

128 lines

Floating reference pixels

Reference Pixels

Pixel to be coded

Reference Pixels (16 bits) + Pixel to be coded (1bit)

Arithmetic Coder → Compressed data

Less outputs for correct prediction

Accurate prediction leads efficient compression
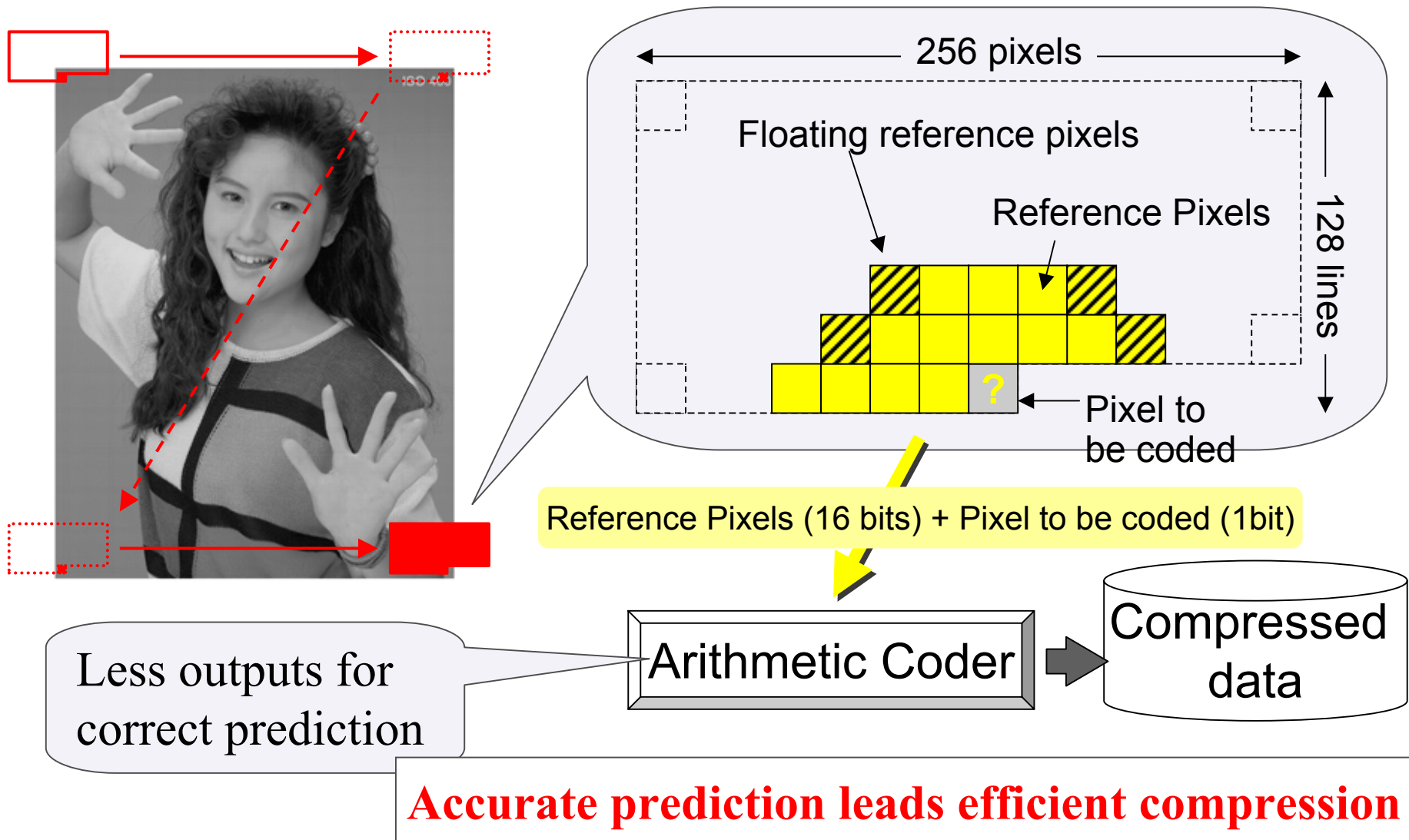
Principle of JBIG2-AMD2

Prediction Coding
Accuracy of pixel prediction affects compression efficiency.

Template

Arithmetic Coder

Compressed data

Pixel to be encoded

Floating reference pixel
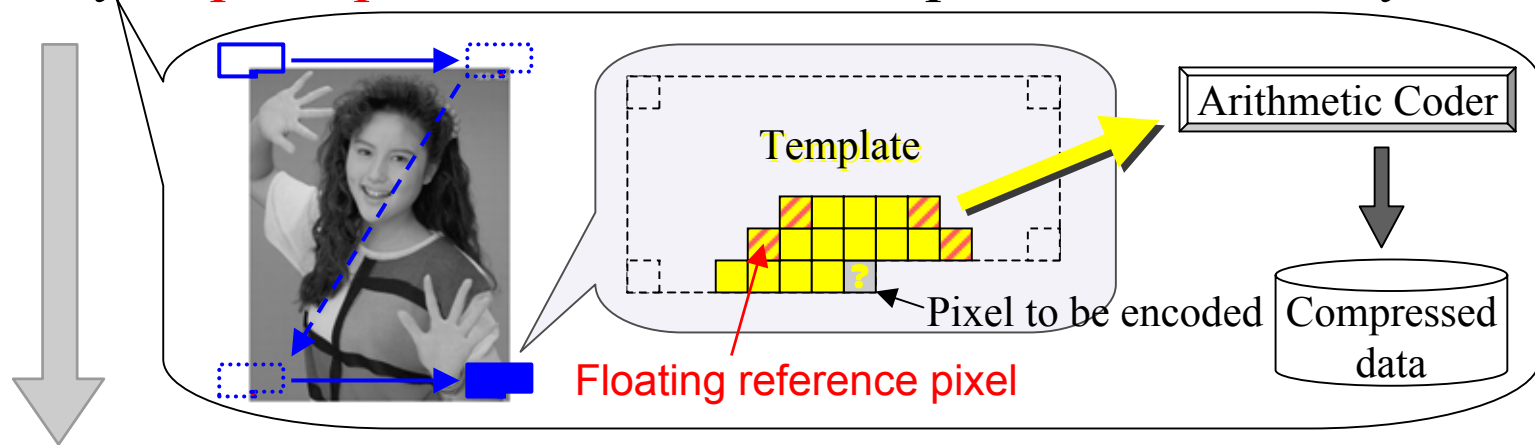
Halftone image with very high-resolution
Conventional methods achieve low prediction-hit rate.
=> Poor compression efficiency

JBIG2-AMD2
Extended template with many floating reference pixels
=> Improved compression efficiency

Structure of graphic-arts image
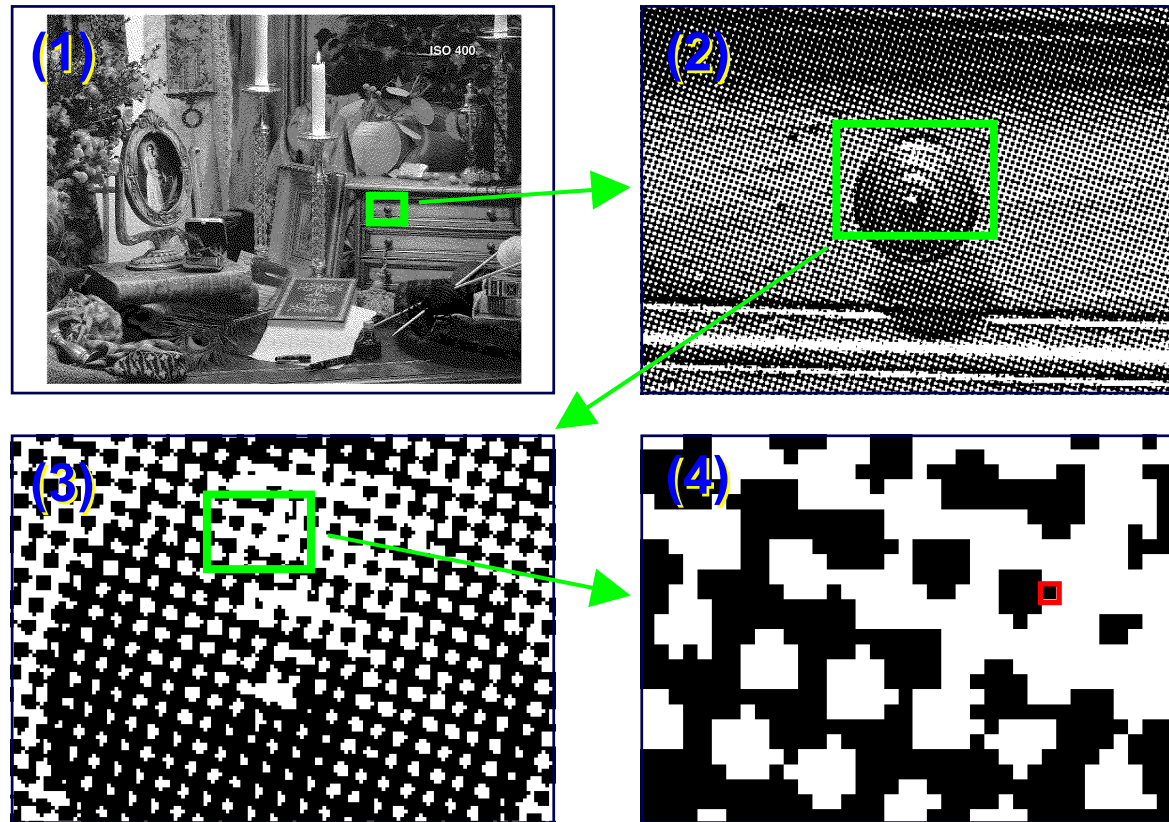
Strange structure: Shading is represented by size of dots, and
Dots' size is represented by density of pixels.

=>Conventional lossless compression method cannot compress well

Limitation of JBIG2

Discovery by AIST:

- Too few floating reference pixels
  - Proposal to ISO: Enhancement of JBIG2
  - Extended template: Increased number of floating reference pixels from 4 to 12
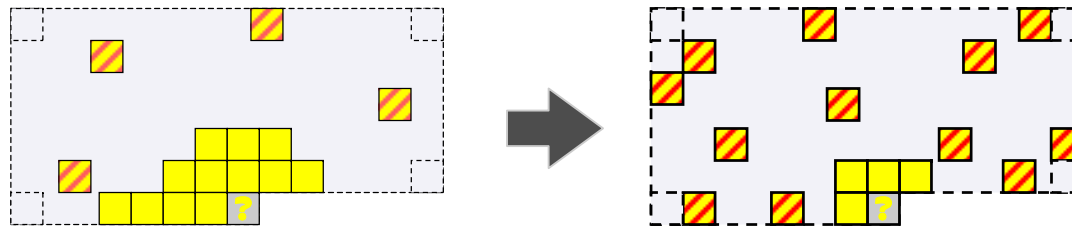
- Large costs for template optimization
  - GA can quickly find the good template configuration for higher compression ratio

AIST method

Genetic Algorithm optimizes the template for the target image data to achieve the higher compression ratio.
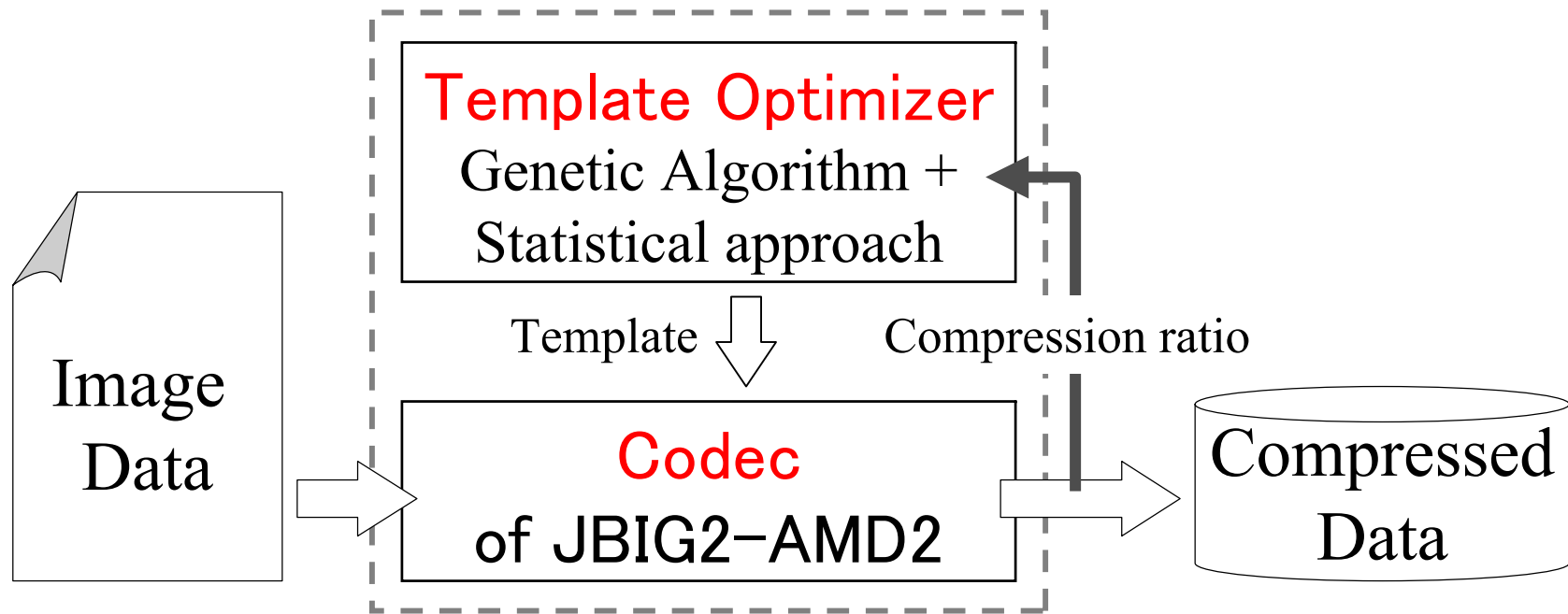
Experimental Results
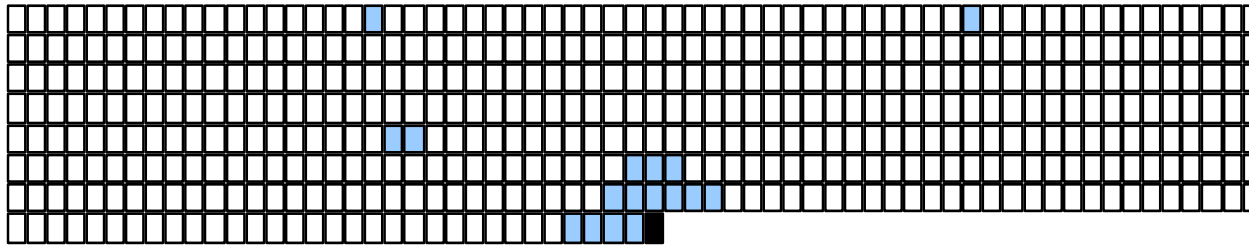
(a) 4 floating reference pixels
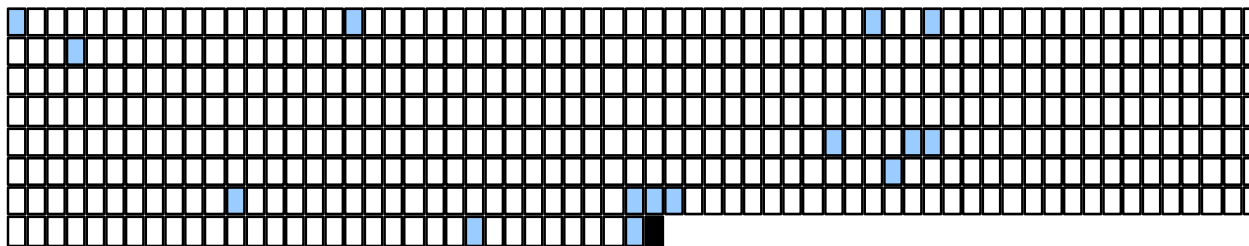
(b) 16 floating reference pixels

More floating reference pixels leads **30%** better comp. efficiency.

- Limitation of JBIG2: Increased floating reference pixels
- Configuration of floating reference pixels
    => Artificial intelligence (AI) techniques

Performance 1 --Compression Ratio--

| Image | | | MMR(G4) | ZIP | JBIG2 | |
SCID#	Angle	Res.			base	AMD2
N5	15	1200	2.36	2.37	8.20	9.10
		2400	3.59	2.74	10.80	13.47
		3600	5.26	3.11	14.95	18.68
	75	1200	2.71	3.56	8.12	9.00
		2400	4.21	4.37	10.30	11.98
		3600	5.58	5.73	15.24	17.91
N6	15	1200	2.14	2.44	9.04	10.26
		2400	3.28	2.75	11.54	14.45
		3600	4.14	2.92	15.47	19.40
	75	1200	2.53	4.64	10.59	11.89
		2400	3.93	5.22	11.98	14.25
		3600	5.03	6.79	16.72	20.06
N8	15	1200	1.78	2.17	5.23	6.14
		2400	2.66	2.39	7.38	9.09
		3600	3.32	2.77	10.88	13.49
	75	1200	2.13	3.49	7.19	7.93
		2400	3.26	4.10	8.56	10.04
		3600	4.06	5.44	13.19	15.79

- **Compression Ratio** = [Original size] / [Compressed size]
- Test data are created by RIPing images in SCID.

Performance 2 (European newspaper)

- 1270 dpi
- 17416 x 27958 pixels
- Approx. 58MB x (CMYK)

Method	CR
G4 Fax	27.67
JBIG1	41.54
This method	60.85

CR (Compression Ratio) =
[Original size] / [Compressed size]

Performance 3 (Book page)
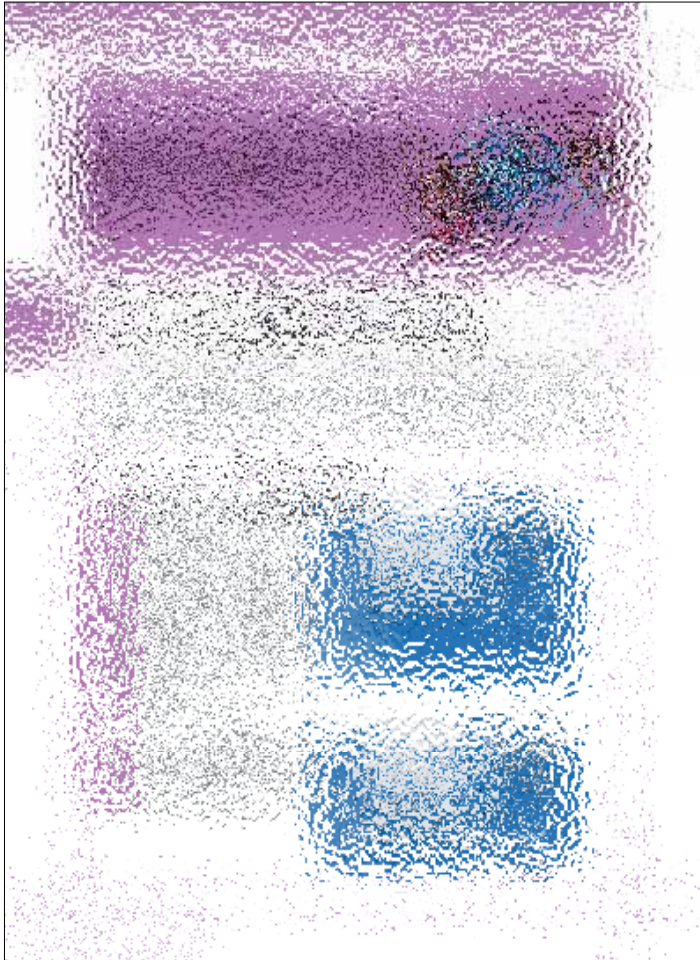
- 2400 dpi
- 17167 x 22100 pixels
- Approx. 45MB x 4 (CMYK)

Method	CR
LHA	28.3
TIFF (LZW)	17.9
This method	120.6

CR (Compression Ratio) =
[Original size] / [Compressed size]

Performance 4 (Leaflet)

- 2400 dpi
- 20400 x 28034 pixels
- Approx. 68MB x 4 (CMYK)

Method	CR
LHA	5.74
TIFF (LZW)	4.69
This method	16.86

CR (Compression Ratio) =
[Original size] / [Compressed size]

Future Plans

- Standardization activity
  - TIFF/IT: Tag Image File Format for Image Technology (ISO 12639)
  - NWI proposal at ISO TC130/WG2 meeting
    - NWI = New Work Item

- R&D of graphic-arts technology at AIST venture company
  - Evolvable Systems Research Institute, Inc.

Application

- 1bitTIFF Workflow
- Graphic-arts machinery
  - Digital copier, Printer, CTP setter, DI press, ...
- Embedment in RIP, Printer-driver, and so on.
- Storage and Management of image data after RIP
- Data transfer

Advanced Graphic-arts system

AIST method
（Bi-level image compression）

JBIG2
Amendment
ISO/IEC JTC1/SC29/WG1

TIFF/IT
ISO TC130/WG2
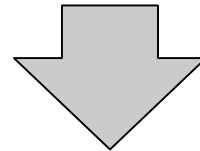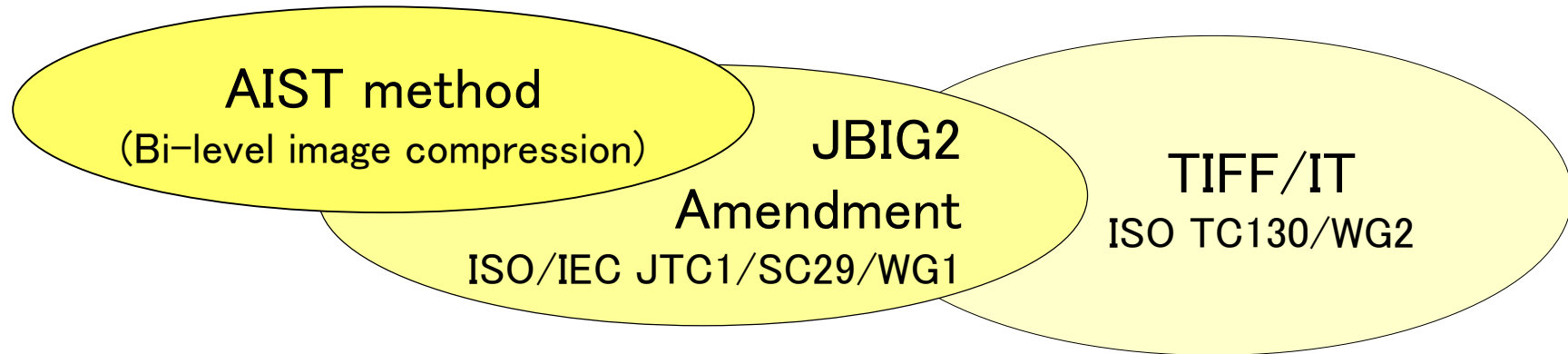
Increase the competitiveness in the graphic-arts industry
in next generation by using AIST method

- CTP (Computer To Plate)setter
- DI (Direct Imaging) Press
- DDCP (Direct Digital Color Proofing)

Target

- World market：46.3 billion dollar (2008)

- Growth at 18%/year

(Prediction of Hidelberg)

CTP (Computer To Plate) Setter

The machine to create *plate*, used in offset press, directly from digital data without analogue film.

Creo Inc.
Trendsetter VLF Quantum

AIST method drastically reduces the costs for data-transfer by efficiently compressing huge graphic-arts image

Leading manufacturer：
Creo, Heidelberg, Fuji Photo Film, Dainippon Screen MFG, Toyo Ink MFG, Toray Industries

DI (Direct Imaging) Press

The press machine with the functionality of laser imaging of thermal plate.
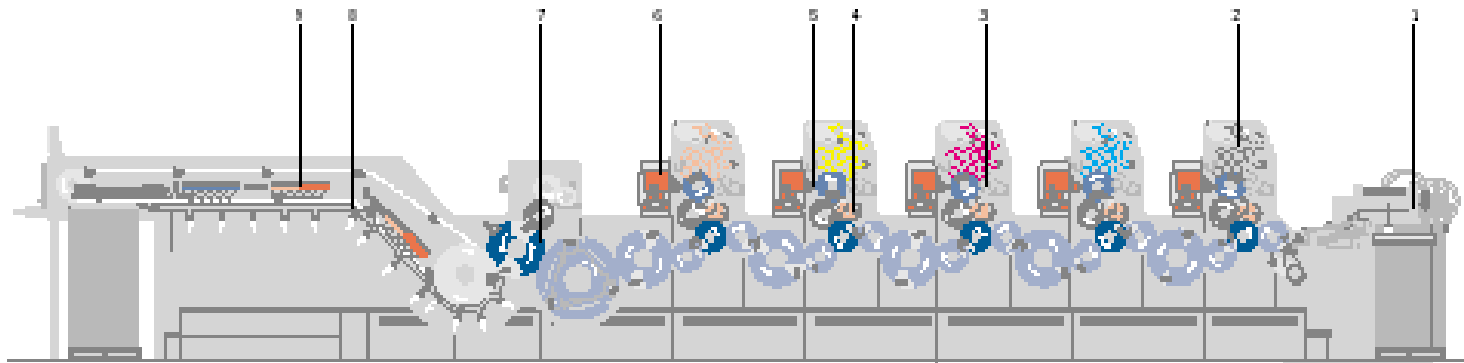
Hidelberg, Speedmaster 74 DI

AIST method drastically reduces the costs for data-transfer by efficiently compressing huge graphic-arts image

Leading manufacturer：
Hidelberg, Adast, Karat Digital Press, MAN Roland, KOMORI, Dainippon Screen MFG, SAKURAI Graphic Systems, RYOBI Imagix

Digital workflow and AIST method

Advantages of digital printing

- Short-run, Low-cost
- Fine precision printing
- Eradication of out-of-print and -existence

The Problem

Enormous size of the image with high-resolution
=> Large costs for transfer and storage
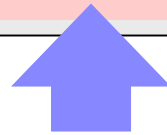
Advantages of AIST method

- Efficient Compression
- Improvement in Compatibility between systems

Target in Graphic-Arts Industry

Large benefit: Total system
Small benefit: Elements in total system

Total system = Workflow
(Author - Edit - Proof - Output - Bookbinding - Delivery)

AIST method

Advanced Workflow for Digital Publishing

FilingPro*
(Image data filing software)

DDCP
(Direct Digital Color Proof)

- CTP
- DI
(Digital Press Machinery)

On-demand
Publishing

*Evolvable Systems Research Institute Inc.

FilingPro (Image Data Filing Software)

[This lossless compression method] + [Database system]

Contents of this talk

- Basic Concept of Evolvable Hardware
- Digital Hardware Evolution
  - Gate-level Evolvable Hardware
    - EMG prosthetic hand
    - Clock-timing adjustment
    - Data compression for print image data
  - Function-level Evolvable Hardware
    - Autonomously reconfigurable neural network chip
- Analogue Hardware Evolution
  - Analogue EHW chip for cellular phones
- Mechanical Hardware Evolution
  - Evolvable Femto-second Laser System
  - Evolvable Interferometer
  - Evolutionary fiber alignment

Function Level Hardware Evolution:
Evolvable Neural Net Chip

- On-line digital EHW

- Purpose
  - fast and autonomous synthesis of non-linear functions
  - time-varying applications like pattern recognition, time-series prediction, etc.
  - Development of dedicated LSI

Problems of Neural Network

- Need of On-line Learning for time-varying applications
- Hardware support for fast NN execution
- Performance of NN
  - heavily depends on the number of hidden layers, hidden nodes, and functions of hidden nodes.

Weak theoretical background,
Limit of hardware support

- Weak performance of On-line learning

RBF vs. Sigmoid function

- Radial Basis Function (RBF) Network
  - fast learning speed
  - large number of hidden nodes

RBF
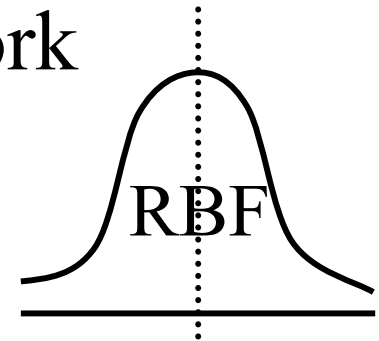
- Sigmoid Neural Network
  - slow learning speed
  - less number of hidden nodes

Sigmoid Function
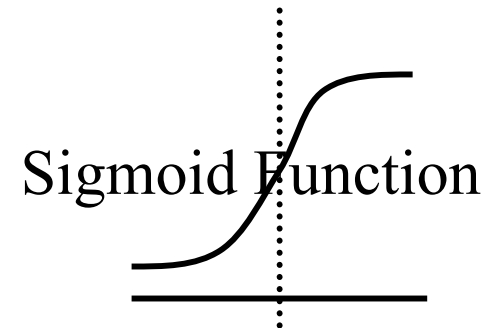
→ Combination of RBF and Sigmoid in single neural network
(Hybrid Neural Network : HNN)

GRD chip: basic concept

Chromosome

(S,c1,d1,w1) (G,a2,b2,w2)

Genetic Operations

(G,a1,b1,w1) (G,a2,b2,w2)
••• (S,ci,di,wi)••• (G,a15,b15,w15)

Network

w1   w2
c1,d1   a2,b2

Sigmoid   Gaussian

x1 x2   xd

Evolution

w1   w15
a1,b1   a2,b2   w2   ci,di   a15,b15

x1 x2   xd

GRDchip

RISC

DSP

+

Reconfiguration

RISC

+

x1x2 •••
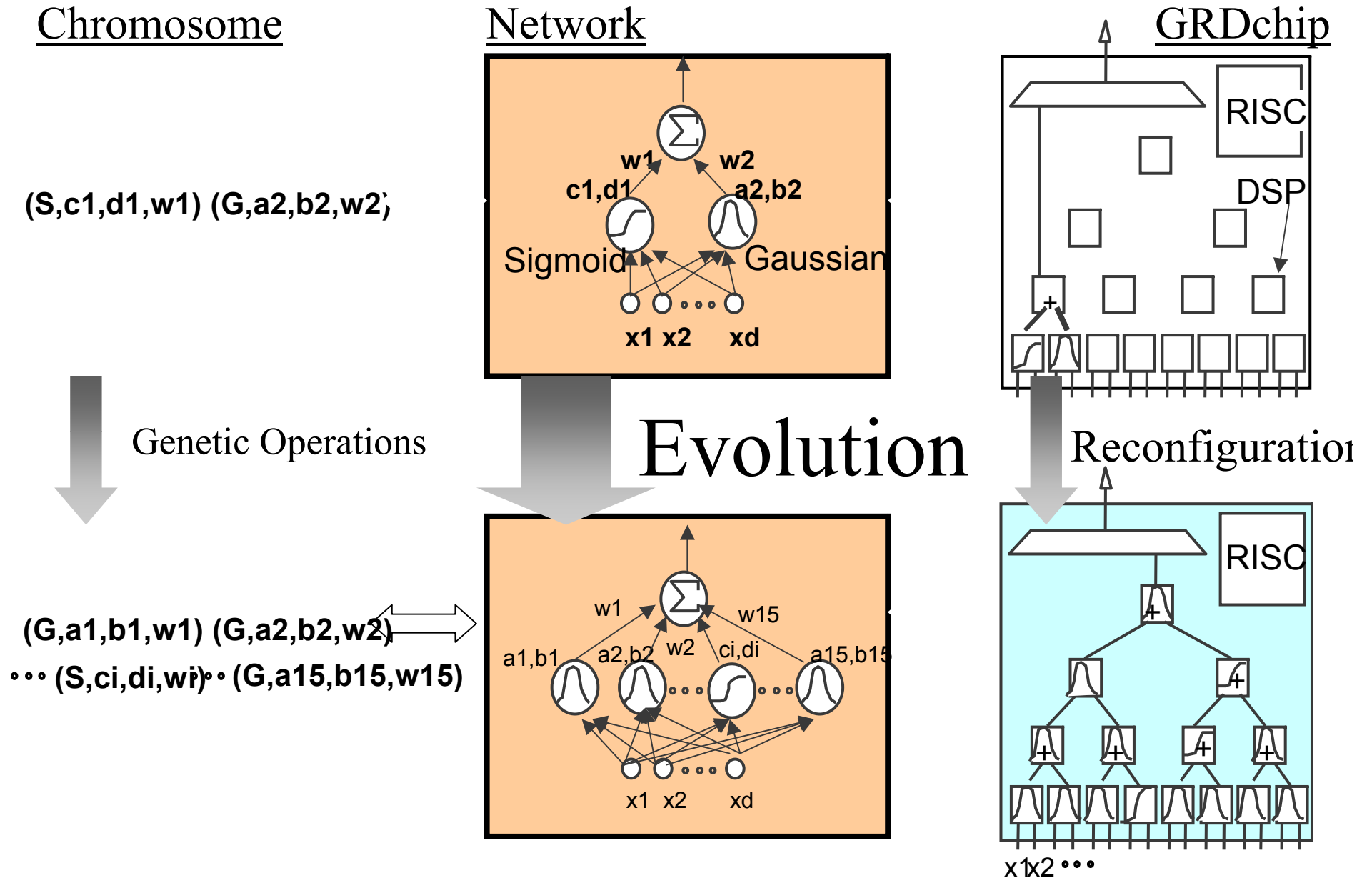
Genetic Reconfiguration of DSPs Chip (GRD chip)
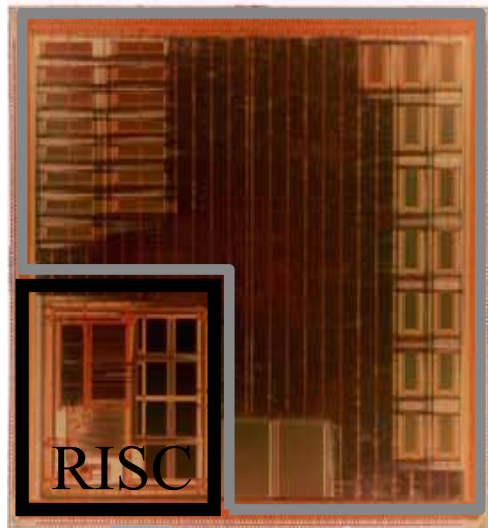
RISC

reconfiguration

(13.5mm x 13.5mm)

- Autonomously reconfigurable Neural Network chip

- 100Mhz 32bit RISC core + 33Mhz 16bit DSP x 15

  – RISC : GA, reconfiguration, I/O

  – DSP : execution of NN,Steepest Descent Method

  – scalable connection of the chips

DSP organization
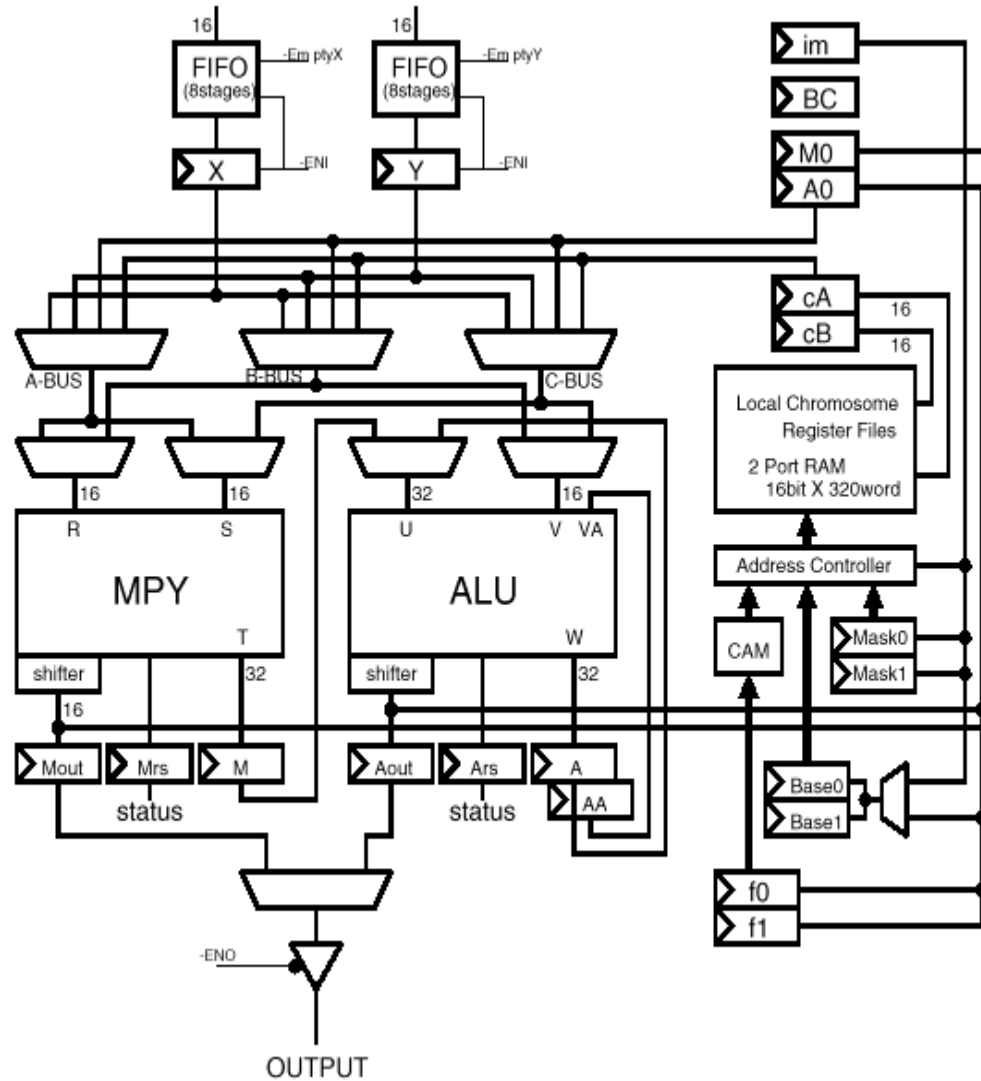
Genetic Learning

- optimal number of hidden nodes, optimal combinations of RBF and sigmoid
  - can not be decided theoretically in advance.
  - Dynamic decision depending on problems and hardware resource.

- Dynamic decision with GA

Performance of GRD chip

- Operational since last June
- second version in progress
- 10 times faster than Pentium II (400MHz)
- 200 times faster than SUN Ultra2
  (with 9 GRD chips)
  - Execution speed per chip
    319MCPS (Mega Connection Per Second)

Adaptive Equalization
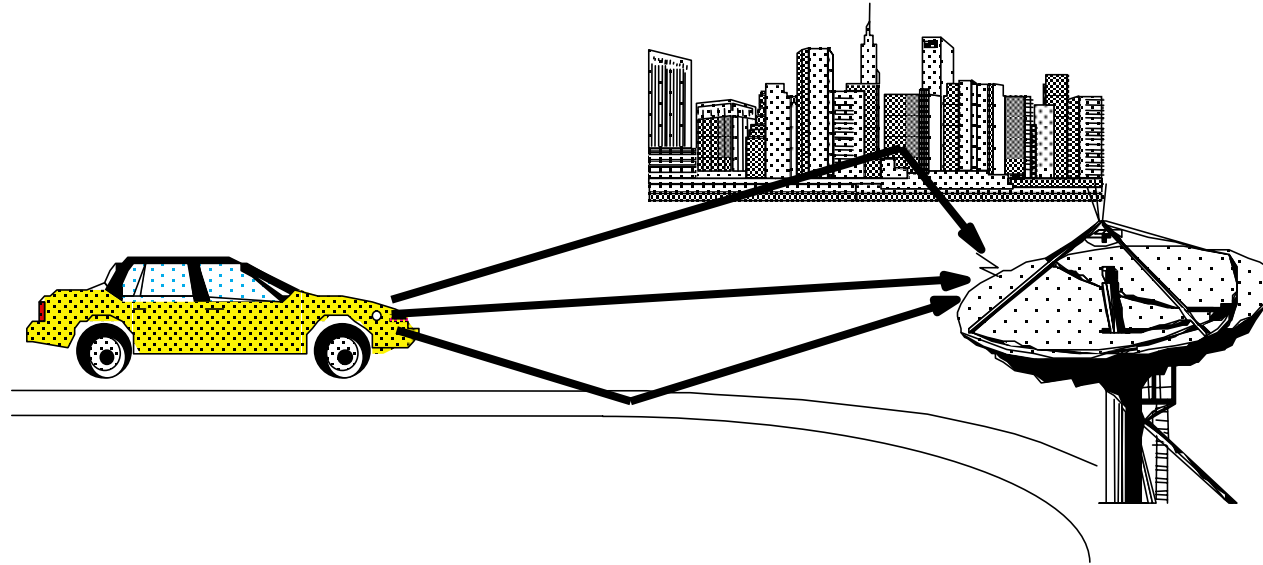
- Adaptive Equalization
  - On-line learning is needed to adapt to the changing environment.
- Fast speed and compact implementation by hardware.

Problems with traditional adaptive equalizer
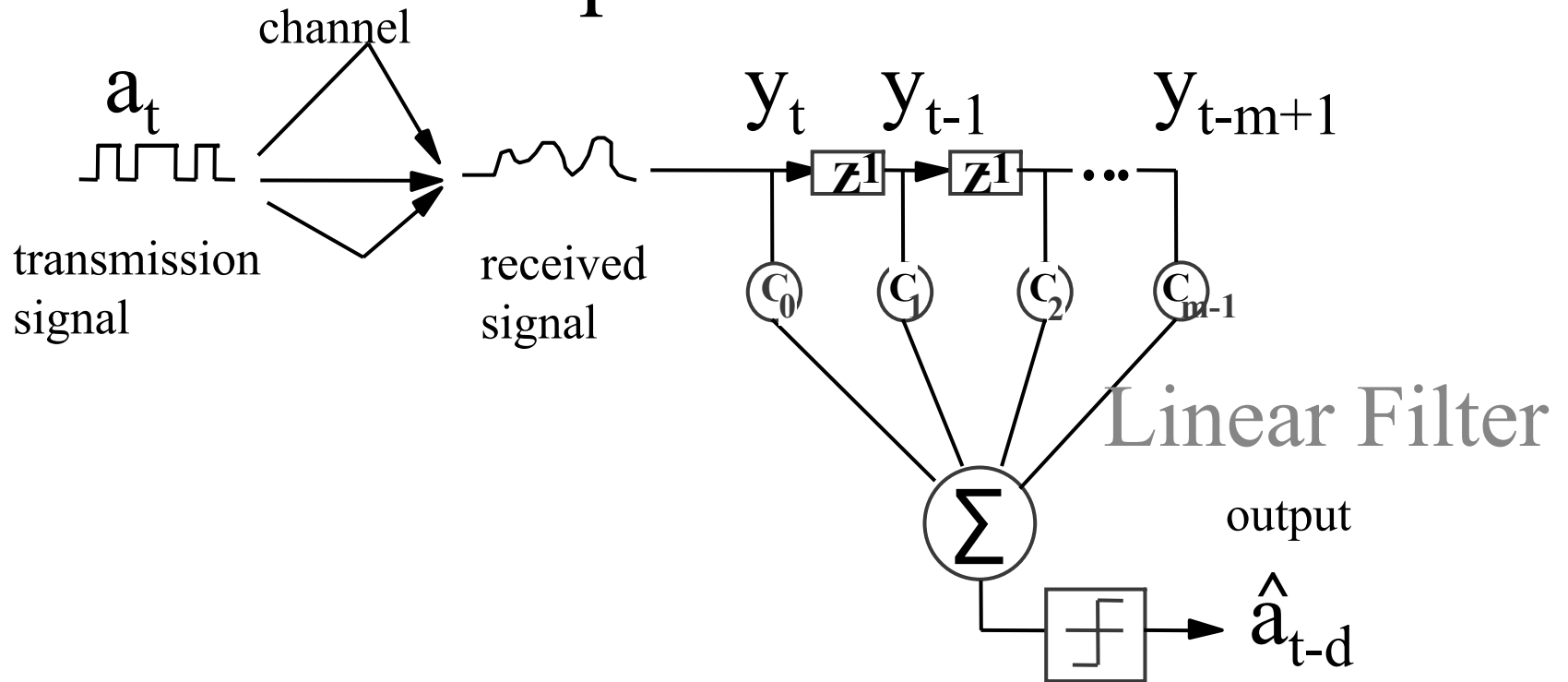
Severe performance degradation when non-linearlity is strong.

Adaptive Equalizer with GRD
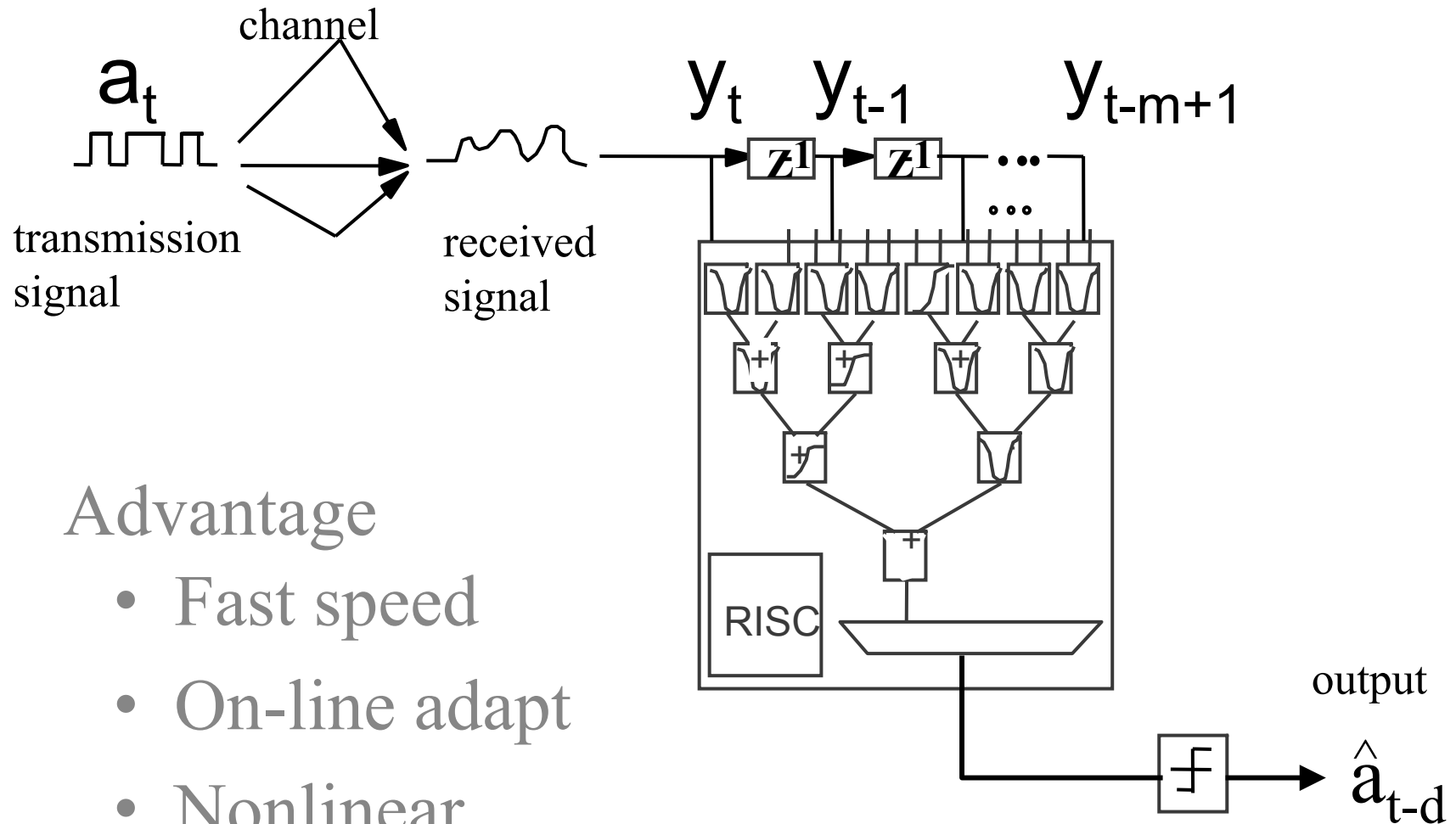
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Analogue EHW chip for cellular phones

- Off-line analogue EHW
- Intermediate Frequency Filter
  – Analogue Band-pass Filter
  – Must be compact and fast: LSI required
  – Large market
- Variations in analogue components performance are adjusted by GA.
- **Installed in cellular phones since Dec. 2001.**

Variations in Analogue Components Values

- Analogue components values can be made as the same as the design specifications.
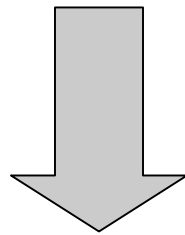
- Yield rates are degraded in high end applications.
  - e.g. Even 1% shift from the center frequency is not allowed in cellular phones.

Off-line analogue EHW chip

- The performance of the analogue EHW chip can be adjusted by downloading adequate bit string (i.e. chromosomes).

- GA reconfigures each chip when it's shipped out.

- Why? To let each chip to fill out the design specification.

Advantages of analogue EHW

- Improvement of yield rate(100%)
- Reduction of die space (60% less)
  - cheaper process can be utilized.
  - Reduction of power consumption(40% less)
- Less effort in the design phase

⟶ Applicable to large variety of analogue circuits.

Analogue EHW chip for IF filter
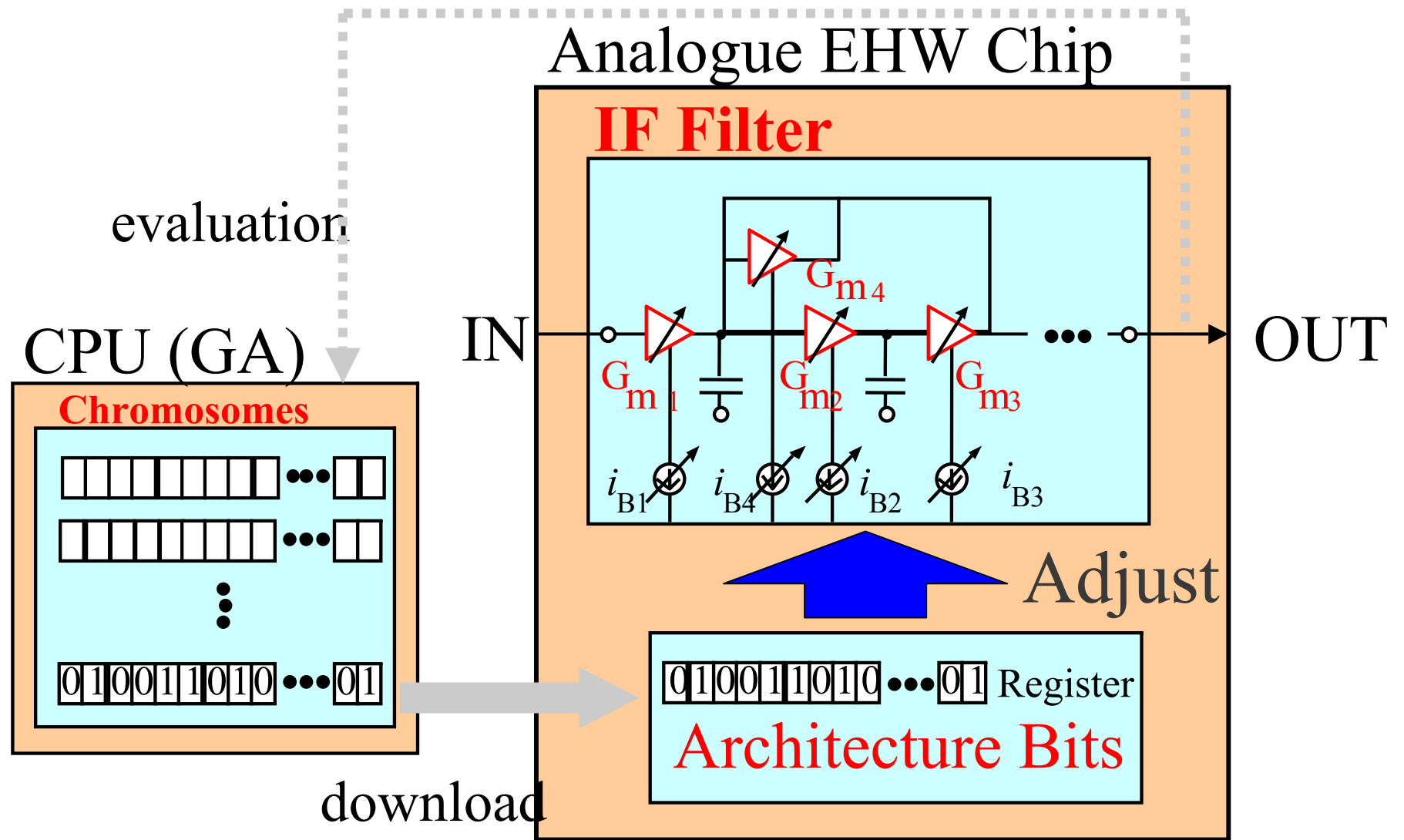
Variation in Gm element

I_B (Bias current)

V_{OUT}

V_{IN}
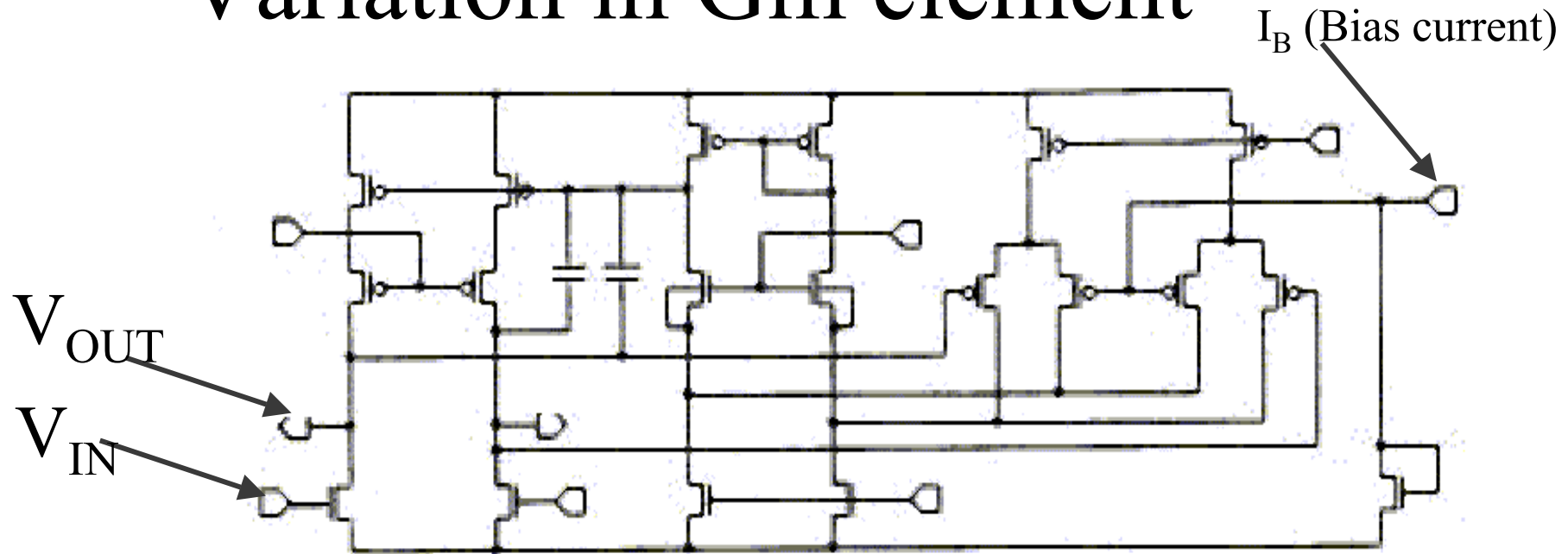
- Gm value (I_{OUT}/V_{IN}) alters 20% (max).
- No chip satisfies the specification without adjustments.

➡️ GA adjusts bias currents:
90% of chips can fill out the specification.

Analogue EHW chip for cellular phones

Bias Current Controller

Filter 1

Filter 2

Filter 3

3.5mm

4.5mm

Result (1)

After   Specification

Gain

Before
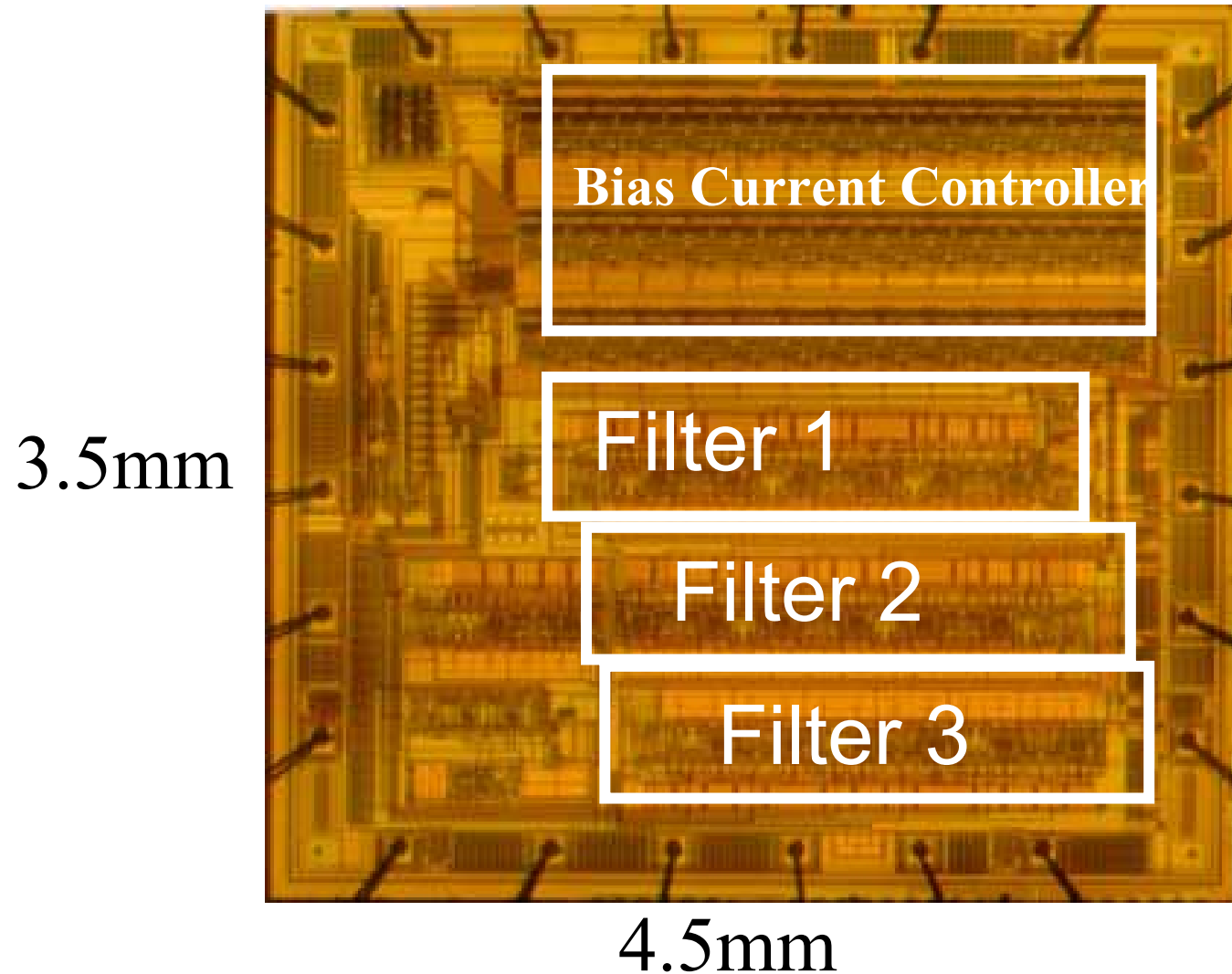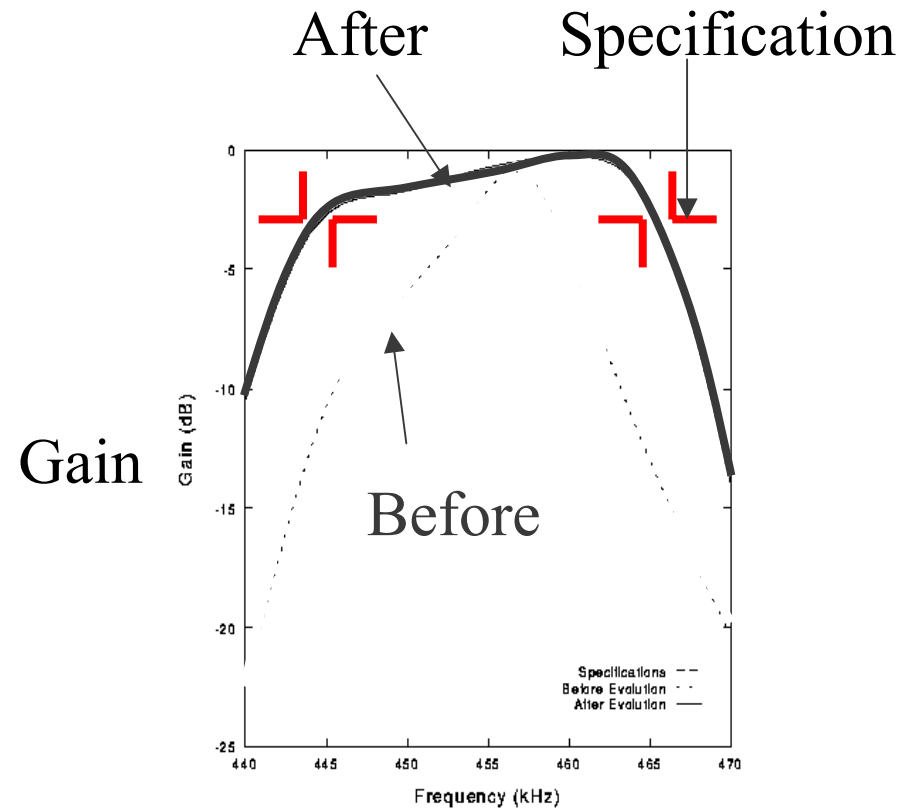
Frequency response

Yield rate : 100 %

Result (2)

- Comparison with other methods
  - hill climbing : 65%
  - GA   : 100%

➡ GA escapes from local minimum.

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Evolvable Femtosecond Laser System

Laser alignment can be optimized autonomously
by genetic algorithms to obtain the maximum output
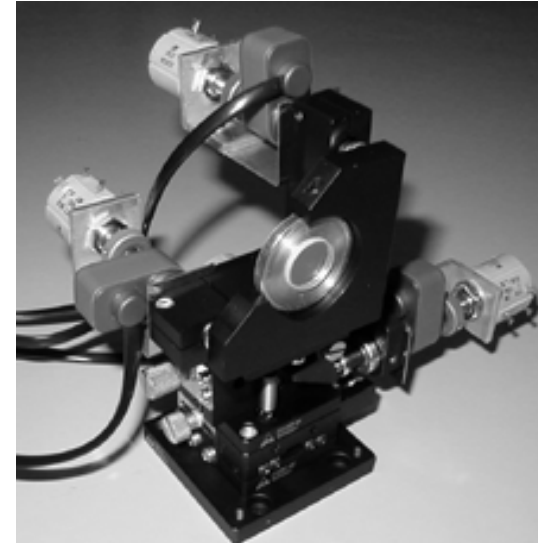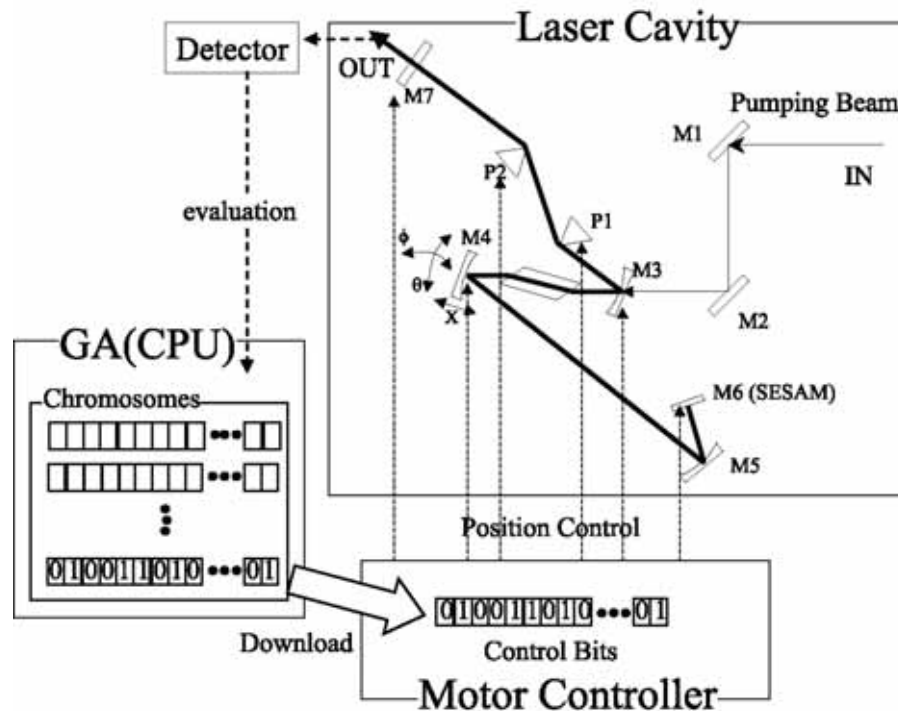
Advantages:
1. Autonomous Adjustment
2. Portable Size
3. Ultrashort pulse ($\sim 10^{-15}$sec)

Especially Suitable for
1. Laser Processing for Diamonds and Shape-memory-alloy
2. Medical Treatment (e.g. macula, depilation)

Interferometer System

- Interferometer is main system of environmental spectroscopic analysis instruments
  - such as Fourier-transform Infrared Spectroscopy(FTIR)
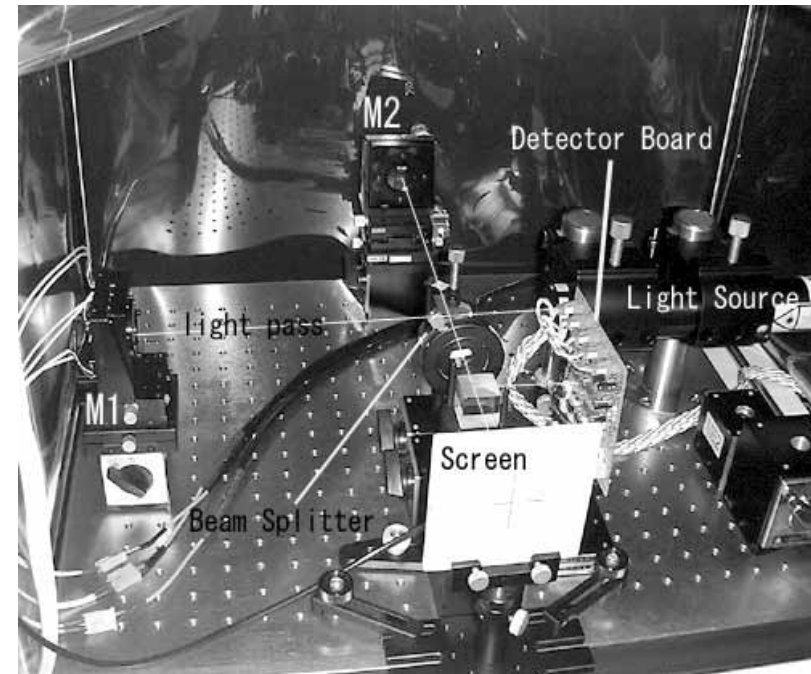
• These instruments are very large, and performance is greatly influenced by environmental conditions.

–Because the internal interferometer have many optical components to necessary precise positioning alignment.
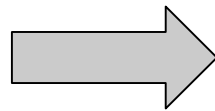
Evolvable Interferometer

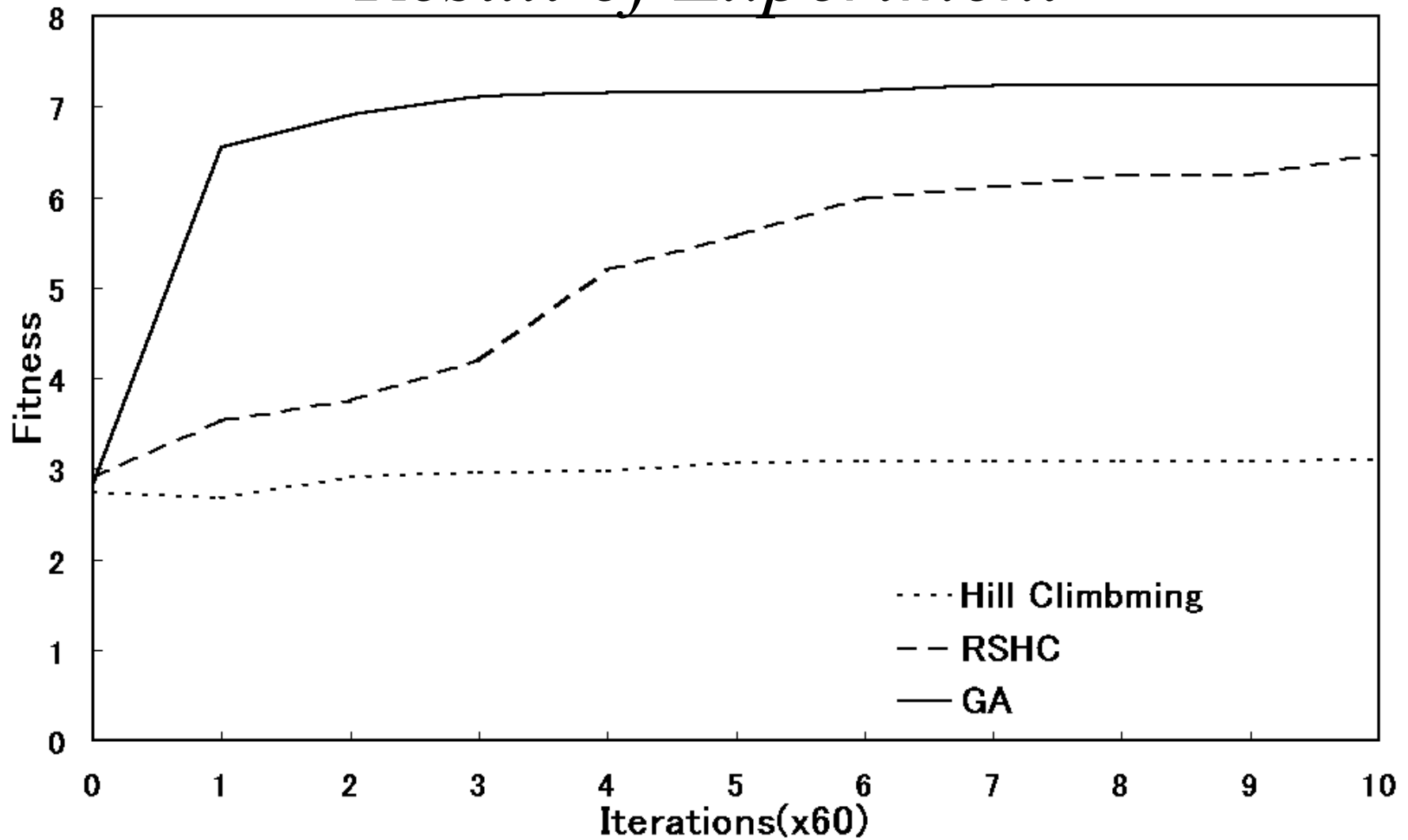- The on-site use of spectrum-analysis instruments has been virtually impossible.
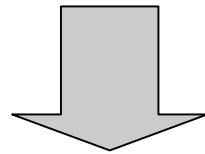
⬅ Automatic Alignment System by GAs

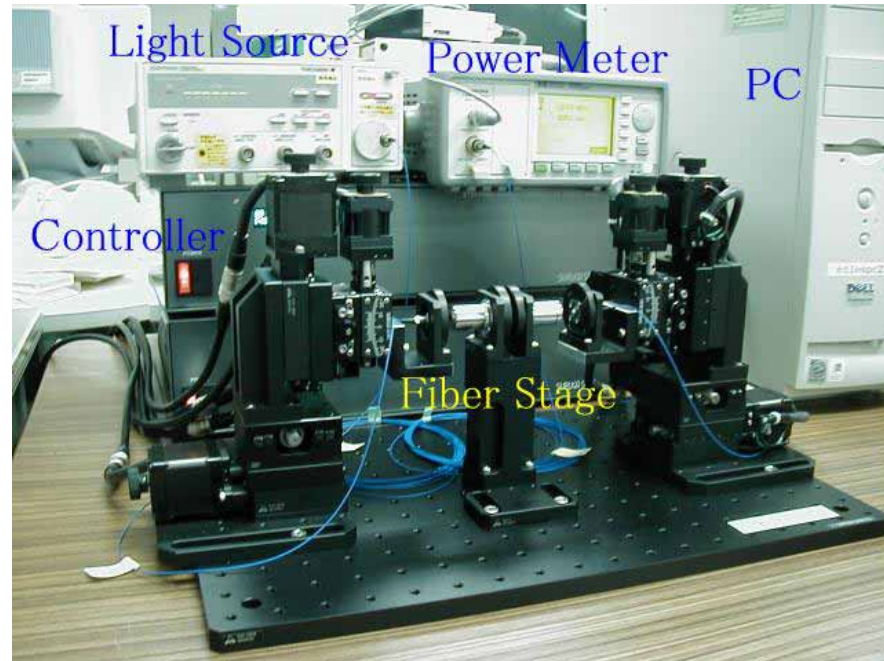- The automatic adjustment method eliminates this problem making it possible to use interferometers outdoors.

➡ The FTIR is used outdoor for environmental analysis *on-site*.

Result of Experiment

Fiber Alignment System
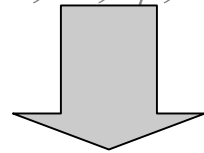
- Fiber alignment is necessary when two optical fibers are connected.

- The connection requires much greater precision in the order of sub-micron-meters.
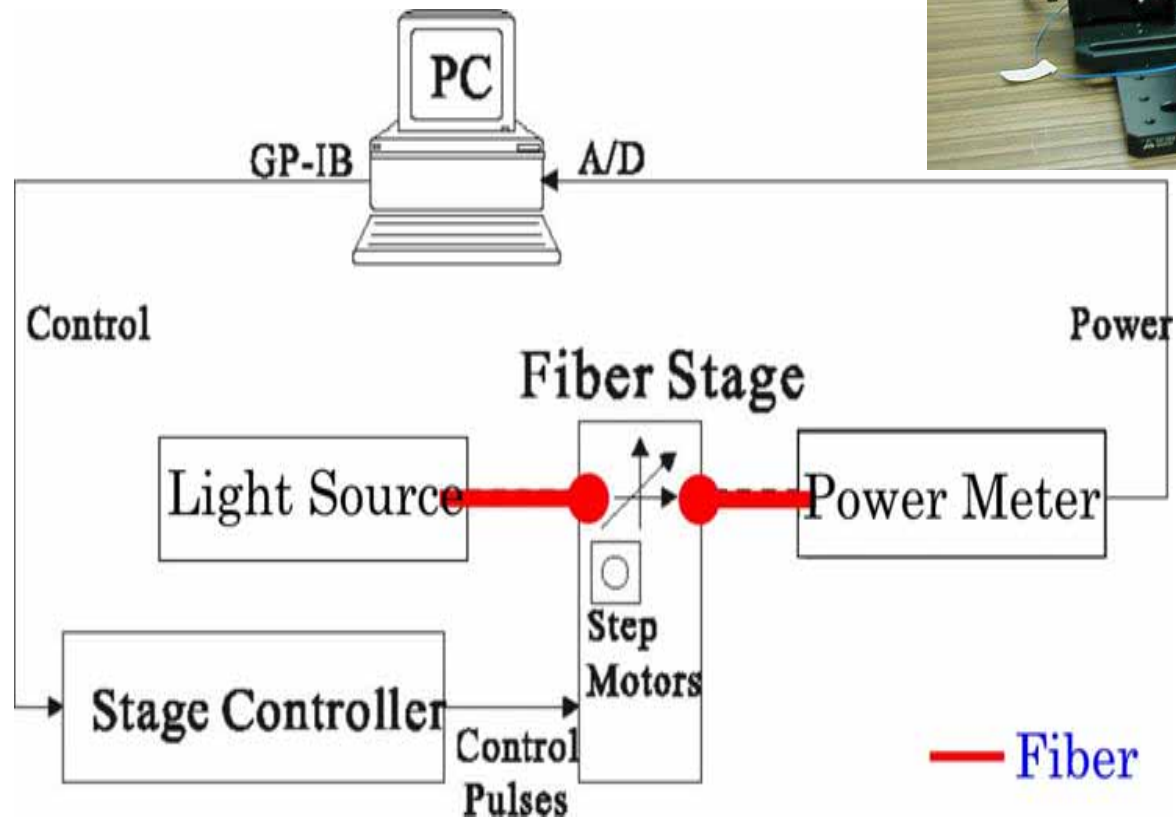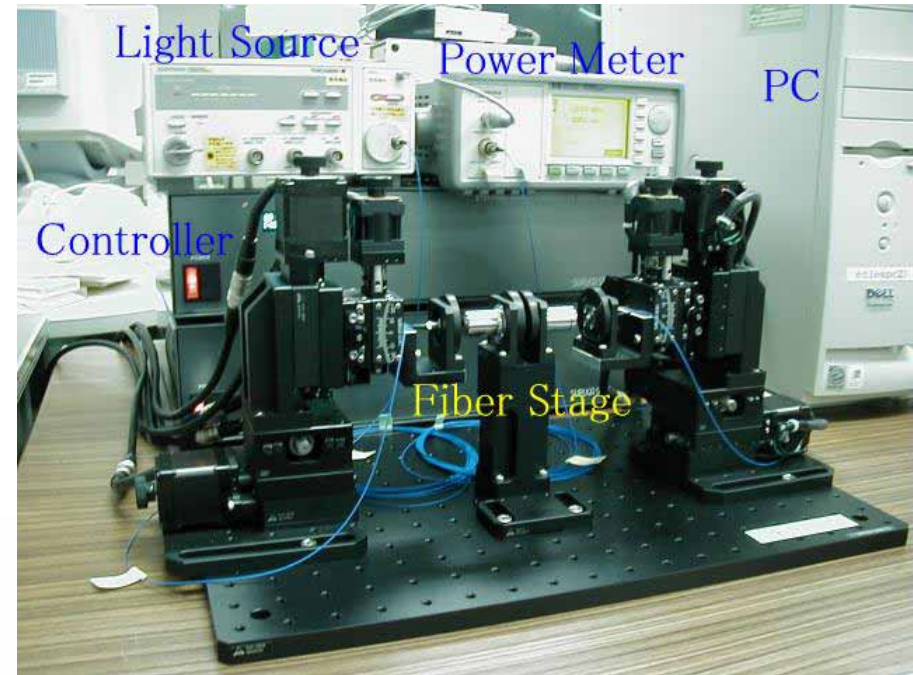
Evolvable Fiber Alignment System

- Conventional fiber alignment system is
  - only capable of fibers with three degree of freedom (x,y,z)
  - non-useful to five or more degree of freedom (x,y,z, θ, ϕ, $\cdots$)

Automatic Alignment System by GAs

- The alignment of optical fibers with five degrees of freedom can be completed within a few minutes.

Developed Fiber Alignment System

Conclusion

- Industrial Applications for EHW
  - Time-variant behaviour (Adaptive)
  - Real-time performance
  - Fault-tolerant
  - Analogue systems
- Promising application domains
  - analogue devices
  - optical systems