Extended Abstract: Automated Transfer of Evolutionary Computation Successes to the Evolvable Hardware Domain for Information Superiority Applications

Laurence D. Merkle[1] and Daniel J. Burns[2]

[1] Rose-Hulman Institute of Technology
5500 Wabash Ave., CM-103
Terre Haute, IN 47804, USA
merkle@rose-hulman.edu
WWW home page: http://www.rose-hulman.edu/~merkle
[2] Air Force Research Laboratory, Rome Site
AFRL/IFTC
26 Electronic Parkway
Rome, NY 13441-4514, USA
burnsd@rl.af.mil
WWW home page: http://www.rl.af.mil/rrs/Info_Inst

Abstract. Achieving information superiority often depends on designing, developing, and implementing effective and efficient approximation algorithms for NP-complete problems. Software-based Evolutionary Computation techniques have achieved considerable success in application to specific NP-complete problems, but the transfer of those results to hardware-based solutions has been slow. The Information Institute of the Air Force Research Laboratory is embarking on an effort to develop tools and techniques to facilitate implementation of algorithmic successes using advanced computing architectures such as Field Programmable Gate Arrays (FPGAs), Field Programmable Transistor Arrays (FPTAs), and hybrids of those architectures with distributed, parallel, and cluster architectures.

One of the top priorities of a modern military commander is "to achieve information superiority over an adversary by controlling the information environment ... The aim of information superiority is to have greater situational awareness and control over the adversary." [1] Achieving greater situational awareness in the modern environment often depends on obtaining good solutions to underlying mathematical problems more quickly than the adversary, so the greatest potential to gain (or lose) information superiority occurs when there are no known efficient and generally applicable algorithms to solve those problems. In particular, when the underlying problem is NP-complete, achieving information superiority depends on the design, development, and implementation of efficient and effective approximation algorithms.

Software-based Evolutionary Computation (EC) techniques have been applied as approximation algorithms for a variety of specific NP-complete problems with considerable success. Unfortunately, the transfer of these results to deployed military systems has been slow in coming, in part because of the limited practicality of efforts to implement them using advanced technologies and architectures such as embedded FPGAs (Field Programmable Logic Arrays), FPTAs (Field Programmable Transistor Arrays), clusters, parallel machines, and heterogeneous approaches (clusters and FPGAs).

The Information Institute within the Air Force Research Laboratory is engaging in an ongoing effort to address this issue by developing techniques to transfer algorithmic successes to the Evolvable Hardware (EH) domain. The specific mathematical problems targeted by this effort are BS (Boolean Satisfiability), TSP (Traveling Salesman Problem), graph partition and coloring, non-linear ordinary differential equation fitting, Bayesian and Artificial Neural Network optimization, and MOPs (Multi-objective Optimization Problems). The development of more effective and efficient solution techniques for these problems will have payoffs in a large variety of military applications, including mobile, agile communications network design with constrained resources; distributed data base design and operation; information packet and vehicle route planning and scheduling; target order sequencing; electronic intelligence signal transmission recognition; radar and hyper-spectral image analysis and clutter rejection filtering; and course of action generation and evaluation.

To the extent possible, this effort will leverage emerging academic and commercial mechanisms to facilitate direct conversion and optimization of existing MatLab and C implementations to the target platforms. For example, it will involve the use of optimizing C compilers that target common or commercially identifiable FPGA platforms, such as Handel-C [2], STREAMS-C [3], SimuLink to VHDL to FPGA [4], and Xilinx "Java-to-Verilog [5] tools. In the process, it will identify limitations of those mechanisms, as well as potential solutions to those limitations. For example, it addresses the implications of choosing specific software/hardware tools (e.g. DSP, FPGA, FPTA), source/target language translation efficiency, and it aims at producing platforms that can easily accept new problem models, as opposed to one particular problem model. Another goal of this effort is to help frame longer term questions regarding the potential for miniaturization and of such computing architectures and possibly about hosting them on minimal platforms and/or distributed networks.

References

1. Information Operations, Air Force Doctrine Document 2-5, 4 January 2002.
2. P. Martin and R. Poli, Crossover Operators for a Hardware Implementation of GP Using FPGAs and Handel-C, 2002 Genetic and Evolutionary Computing Conference (Proceedings), NY, NY, July, 2002, pp. 845-852.
3. STREAMS-C: Developed under DARPA funding under the direction of Maya Gokhale/Los Alamos National Laboratory. Accepts a subset of the C programming language, performs behavioral synthesis, and outputs synthesizable RTL VHDL

code. It currently targets Xilinx Virtex-2000 devices on Annapolis Microsystems' Firebird board, but claims to be easily re-targeted.

4. Simulink-to-VHDL-to FPGA pursued by a partnership between MathWorks and Xilinx. MatLab/Simulink to VHDL to FPGA: targets Xilink's Virtex II Pro XC2VP125, which contains, among other things, four integrated PowerPC cores and 556 individual 18x18-bit multipliers. Further chips provide over 1000 configurable I/O pins. (or XC2V1000-4FG456C FPGA)
5. Xilinx sells a "Java-to-Verilog" converter called "Forge" for $5K.