A 3.8-mW 2.5-GHz Dual-Modulus Prescaler in a 0.8 μm Silicon Bipolar Production Technology

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ABSTRACT

This paper presents a dual-modulus ÷128/÷129 prescaler operating up to 2.5 GHz. It consumes only 3.8 mW from a 2.3 V supply when driving an 8 pF capacitive load. The circuit is operational with supplies ranging from 2 V to over 7 V. With a 2 V supply it consumes only 1.38 mA while still operating up to 2 GHz.

The circuit is manufactured in a standard silicon bipolar production process (Siemens B6HF). This 25 GHz-f_T double-polysilicon technology uses 0.8 μm lithography and LOCOS isolation. The chip is mounted in a 6-pin SOT363 SMD package.

1. INTRODUCTION

The fast-growing mobile communications market causes a demand for small, inexpensive electronic components operating at frequencies in the range of 1 to 2 GHz. Low-power and low-voltage operation are important requirements for these circuits.

Dual modulus prescalers are key parts in the frequency synthesizers used in cordless and cellular phones. Figure 1 shows the block diagram of a typical phase-locked loop (PLL) synthesizer. The output signal of the voltage-controlled oscillator (VCO) is applied to the dual modulus prescaler which acts as a divider by *P* or *(P+1)*, respectively.

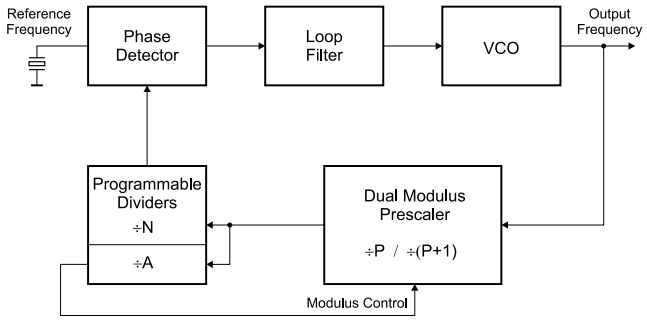

Figure 1: PLL Block Diagram

At the prescaler output the frequency is in a range that can be handled by the following programmable dividers. These divide-by-A / divide-by-N counters are typically contained in a CMOS IC together with the phase detector. The resulting output frequency of the PLL is

$$f_{out} = f_{ref} \cdot ((N \cdot P) + A)$$

Several dual-modulus prescalers operating between 1 and 2 GHz fabricated in silicon bipolar [7],[8], CMOS [2],[3] and CMOS/SIMOX [4] have been published.

It was the goal of this work to design a dual-modulus prescaler that operates up to more than 2 GHz to include the frequency bands used for the DECT, PCS and DCS standards. Main demands were operation with a supply ranging from below 2.7 V to at least 5.5 V and extremely low power dissipation. Since it was decided to mount the chip in a tiny SOT363 SMD package, which measures only approximately 1.25 mm by 2 mm, the chip size was also restricted. The SOT363 package has six pins. Two of these are internally connected and used for ground. The remaining pins are needed for Vcc, Input, Output and Modulus Control. This means that a differential input found in many circuits [7],[8] or a selection of different divider ratios (e.g. ÷64/÷65 and ÷128/÷129) is not possible due to the limited number of pins.

2. CIRCUIT DESIGN

The prescaler consists of a synchronous divide-by-4 / divide-by-5 input stage and a 5-stage asynchronous divider (fig. 2). All outputs of the asynchronous divider and the modulus control (MC) input are connected to an OR gate. When all divider outputs and the modulus control input are LOW, the output of the OR gate becomes LOW, which in turn causes the input stage to divide by 5 once. The resulting overall division ratio therefore becomes 129. When MC is LOW the input stage always divides by 4 and the overall ratio is 128.

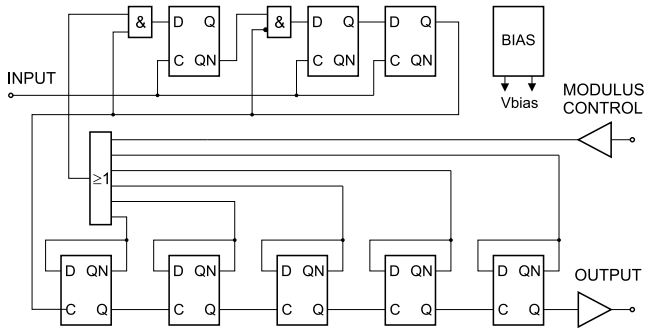

Figure 2: Schematic Diagram of the Prescaler

The prescaler is implemented in fully differential current mode logic (CML). The fully differential operation allows a reduction of the internal voltage swing to only 200 mV while maintaining a sufficient noise margin. This small voltage swing increases the speed of operation of the circuit and allows operation with a reduced supply voltage.

To obtain a constant swing with supplies ranging from 2.3 V to 7 V the bias voltage for the current sources used in the gates and flip-flops has to be kept constant. This is accomplished by a bias network which provides a bias voltage that is compensated against variations of the supply voltage and the ambient temperature.

2.1 Input

Due to the limited number of pins available in the SMD package intended for mounting the chip only a single-ended input is possible. The conversion from a single-ended input signal to the differential signal needed by the internal circuitry is done by using on-chip bypassing capacitors. The value of these capacitors is a compromise between the lowest possible operating frequency which requires large capacitors and the available chip area. The capacitors used in this design have a total capacitance of 8 pF and require an area of approximately 5000 μm^2.

2.2 Divider-by-4/5

The divider ÷4/5 is formed by three D-type flip-flops and two AND gates. The flip-flops consist of a master and an identical slave section. The master output is connected to the input of the slave, whereas the slave clock is the inverted master clock. Figure 3 shows the schematic diagram.

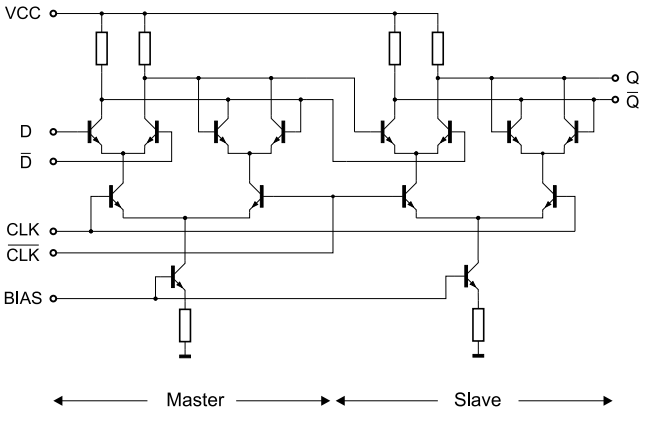

Figure 3: Master-Slave Flip-Flop

All three flip-flops are clocked with the input frequency. They determine the maximum operating frequency of the prescaler and draw the main part of the supply current. This can be seen in figure 4 which shows the contribution of the different sections of the prescaler to the current consumption. The divider-by-4/5 consumes 52% of the total current. Careful optimization of the divider ÷4/5 is therefore necessary to achieve low-power operation of the prescaler.

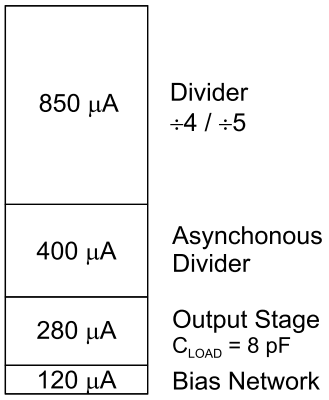

Figure 4: Distribution of the Supply Current

2.3 Asynchronous Divider

The asynchronous divider consists of five flip-flops. Since the maximum frequency is already lower by a factor of four than at the prescaler input the operating current of these flip-flops can be reduced accordingly. The last three flip-flops in the divider operate at a current of 16 µA each. These flip-flops would still operate up to the required frequency with a much lower current. However, their increased delay at lower currents would cause an increase of the setup time of the prescaler. This setup time is the time needed for the prescaler to react to a change at the Modulus Control input and to change the divider ratio accordingly.

All flip-flop outputs and the Modulus Control Input are connected to an OR gate. Due to the use of complementary signals only gates with no more than two inputs can be realized when two-level series-gating is used. Therefore this OR gate is implemented by cascading five two-input gates. The Modulus Control input is connected to the OR gate via a level converter. This circuit converts the external control voltage usually coming from a CMOS or TTL circuit to a differential signal with 200 mV swing as needed by the internal circuitry. The threshold was set to 1.5 V to be compatible with both CMOS and TTL circuits.

2.4 Output Driver

The single-ended output has to drive the input of an integrated PLL circuit in most applications. The input of these circuits presents a high impedance capacitive load to the prescaler. The required voltage swing is typically below 1 V_{pp}.

For very low power prescalers the current needed to drive this capacitive load can become a major part of the total current consumption. To generate a voltage swing of ΔV across a capacitance C_L a current of

$$I = \Delta V \cdot C_L \cdot f_{out}$$

is necessary. This current is proportional to the frequency f_{out} at the prescaler output and to the load capacitance C_L. For a voltage swing of 1V, a capacitive load of 8 pF and a frequency of 2.5 GHz / 128 this results in a current of 156 µA. This corresponds to approximately 10% of the total current consumption of this prescaler.

3. TECHNOLOGY

The prescaler is manufactured in the Siemens B6HF silicon bipolar production process [5]. This double-polysilicon, 0.8 µm-lithography, LOCOS-isolated technology features npn transistors with an f_T of 25 GHz, lateral pnp transistors, 3-layer metalization, and linear capacitors.

The prescaler uses only npn transistors in the signal path. Although minimum size transistors (0.8 µm x 1.1 µm emitter mask) were used even in high-frequency sections of the prescaler, they still operate far below their optimum current density. This causes a reduction of their cutoff frequency f_T which poses no problem since the transistors remain fast enough for this application. The upper frequency limit of the prescaler is not determined by the transitor f_T but by the parasitic capacitances of the transistors and wiring. These parasitic capacitances dictate the amount of current needed for a specific operating frequency. Pnp transistors are only used in the bias network where their low f_T is not critical.

The layout was carefully optimized to reduce the length of critical paths and the overall chip size. It uses only two of the three available metalization layers to reduce the production cost of the circuit. The chip measures 480 µm by 350 µm and contains approximately 210 transistors. All inputs and outputs are ESD protected.

4. EXPERIMENTAL RESULTS

All measurements were performed with the packaged prescaler ICs mounted on microstrip boards (see fig. 5).

Figure 6 shows the input sensitivity of the prescaler with the bottom trace indicating the minimum level required for correct operation and the top trace showing the maximum level. The dynamic range exceeds 25 dB over a wide frequency range. For this measurement a 50 Ω resistor is connected from the input of the test board to ground to terminate the signal source. The signal is then ac-coupled to the prescaler IC. The sensitivity is identical for both divider ratios of 128 and 129.

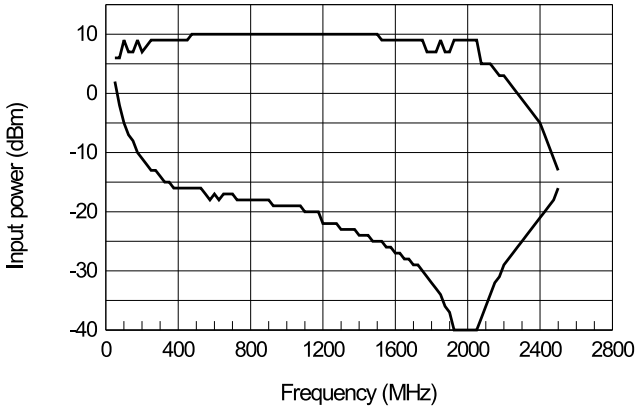

Figure 6: Prescaler Sensitivity

At frequencies below 400 MHz the prescaler needs higher input levels. There are two different effects which cause this behavior. On the one hand the slew rate of the input signal becomes too low at lower frequencies. The zero crossings of the input signal correspond to an illegal logic level between LOW and HIGH. Therefore the transitions between LOW and HIGH (i.e. the slew rate) have to be fast enough to ensure proper operation of the prescaler. On the other hand the on-chip bypassing capacitors in the input stage of the prescaler cause a cut-off frequency of approximately 80 MHz. Measurements show that the prescaler is operating at frequencies down to 40 MHz.

Figure 7 shows the input and output signals for a divider ratio of 128 and 129 respectively. The output voltage swing is $\geq 1\ V_{pp}$ over the entire frequency range.

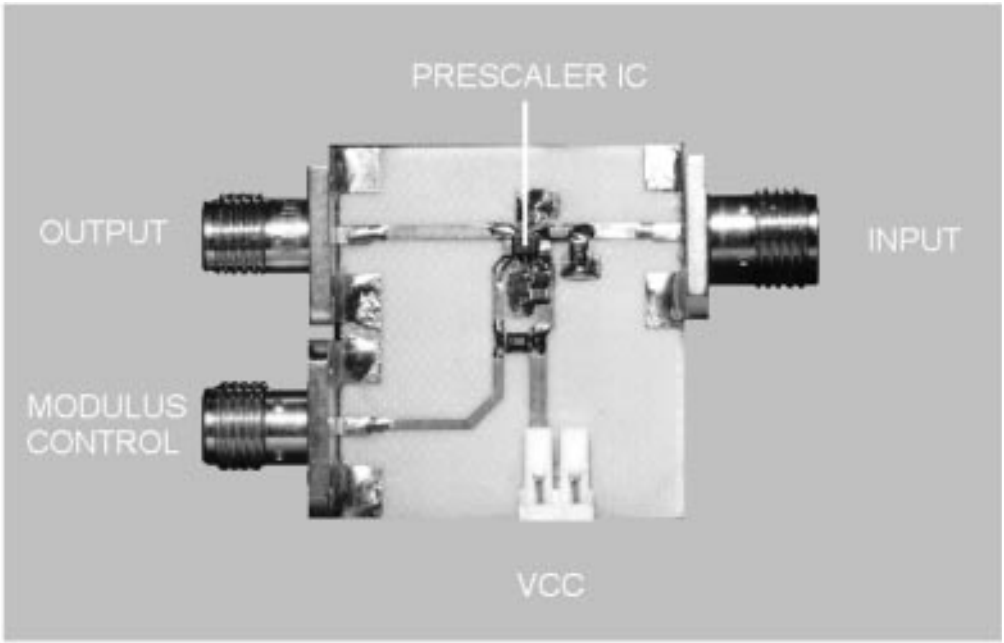

Figure 5: Test Fixture (28 mm x 25 mm)

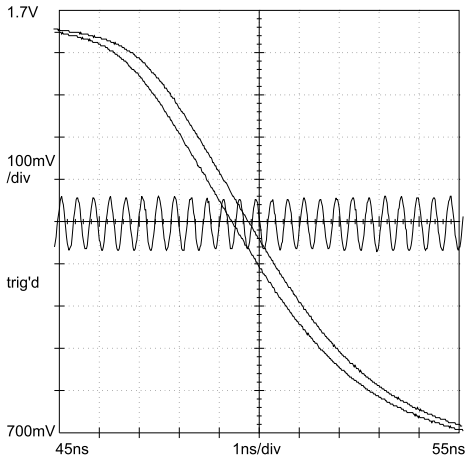

Figure 7: Prescaler Input and Output Signals

Due to the bias network the supply current varies only by approximately 20% for a supply voltage ranging from 2.3 V to 7 V. This in turn means that the maximum operating frequency depends only weakly on the supply voltage. With a 2.3 V supply the prescaler operates up to 2530 MHz and draws 1.65 mA when driving a capacitive load of 8 pF. For a 7 V supply the maximum frequency is 2680 MHz. The prescaler is still functional with supplies of 2 V and below. With a 2 V supply the prescaler operates up to 2 GHz while drawing only 1.38 mA which results in an extremely low power of less than 2.8 mW.

Table 1 gives an overview of the prescaler data and figure 8 shows a comparison with several silicon bipolar and CMOS prescalers that have recently been published.

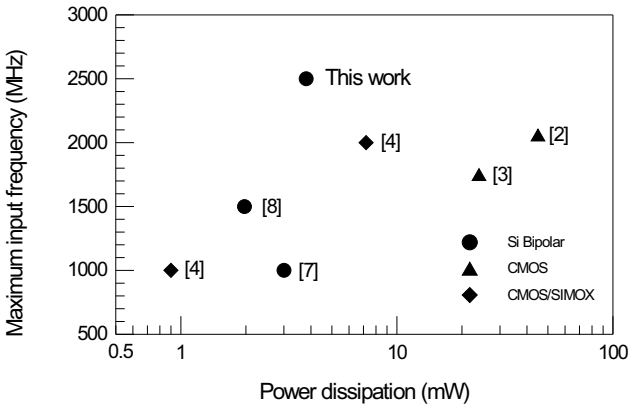

Figure 8: Prescaler Comparison

Supply Voltage	2 V - 7 V
Supply Current (Vcc = 2.3 V)	1.65 mA
Maximum Frequency (Vcc = 2.3 V)	2530 MHz
Output Voltage Swing	1.1 V_{pp}
Setup Time	13 ns
Chip Size	480 x 350 µm

Table 1: Prescaler Data

5. CONCLUSIONS

We have presented a dual-modulus prescaler with extremely low power consumption manufactured in a well-proven silicon bipolar production process. It operates with supplies ranging from 2 V to 7 V. The maximum operating frequency is 2.5 GHz with a 2.3 V supply and a power of only 3.8 mW. The prescaler is intended mainly for applications in mobile communications systems in the 2-GHz range such as DECT, PCS and DCS.

Advances in silicon [1] and SiGe [6] bipolar technologies let us expect a significant reduction in power and increase in speed. Although existing production technologies are fast enough to design prescalers for frequencies of 2 GHz and more, significant reductions in power can be expected from advanced technologies using smaller lithography and improved isolation schemes.

6. REFERENCES

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